SL-C9E/C9UB

OPERATION MANUAL

AEP Model
UK Model
E Model

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MICROFILM

Beta

VIDEO CASSETTE RECORDER

SONY®

Consumer VIDEO

SECTION 1
VIDEO CIRCUIT

GENERAL

The video signal system circuit is on boards RP-7 and RV-7. The RP-7 board contains the recording amp that supplies low-frequency converted chroma signals and Y-FM signals to the video head, the head amp that amplifies the playback signals from the video head, and the head selection circuit. This is the main board in the video system. During E-E and recording time, it outputs video signals unchanged. During recording, the input video signal goes through the AGC circuit of IC003, the chroma signal is removed by the LPF to form the luminance signal, which is sent back to the deviation circuit of IC003. The deviation circuit controls the luminance signal level so that the frequency deviation is 1.4 MHz. The luminance signal deviation is adjusted and clamped by IC019 and given 1/2fH shift, nonlinear pre-emphasis, white clip and dark clip in IC018, then FM modulated in IC015 to form Y-FM signal.

The chroma signal is separated from the luminance signal by the BPF, goes through ACC circuit of IC008, is given a pilot burst signal in IC009, frequency converted in IC012, and combined into a low- frequency converted chroma signal with A field at 685 kHz and B field at 689 kHz. The Y-FM signal and low-frequency converted signal are sent to the RP-7 board for Y/C mixing, and then supplied to the video head.

During playback, the playback signal from the video head goes to the head amp and switching circuit on the RP-7 board for Y/C separation, and then sent to the RV-7 board. The Y-FM signal is limited and FM-demodulated in IC014 and IC015, goes through LPF, non-linear de-emphasis is carried out in IC016 and IC017, crosstalk is removed by the comb filter of IC002, drop-out is compensated, and supplied, via IC003 and the noise canceller in IC019, to the Y/C mixer circuit.

The chroma signal, picked out by the LPF, goes through the ACC circuit in IC008 and through IC009 (not during playback), then its frequency is converted in IC012 to the original 4.43 MHz chroma signal. The 4.43 MHz chroma signal has crosstalk removed by the comb filter, goes, via the chroma phase inverter discriminator in IC008, to IC004 to have the pilot burst removed, and is supplied to the Y/C mixer circuit. During variable speed playback, the IC004 compensates for chroma signal phase inversion caused by track motion of the video head and replaces the burst signal by a sub-burst signal.

The signal being Y/C mixed in IC019, is output as a playback video signal. During variable speed playback, a quasi VD is inserted in IC021.

VIDEO SYSTEM BLOCK DIAGRAM

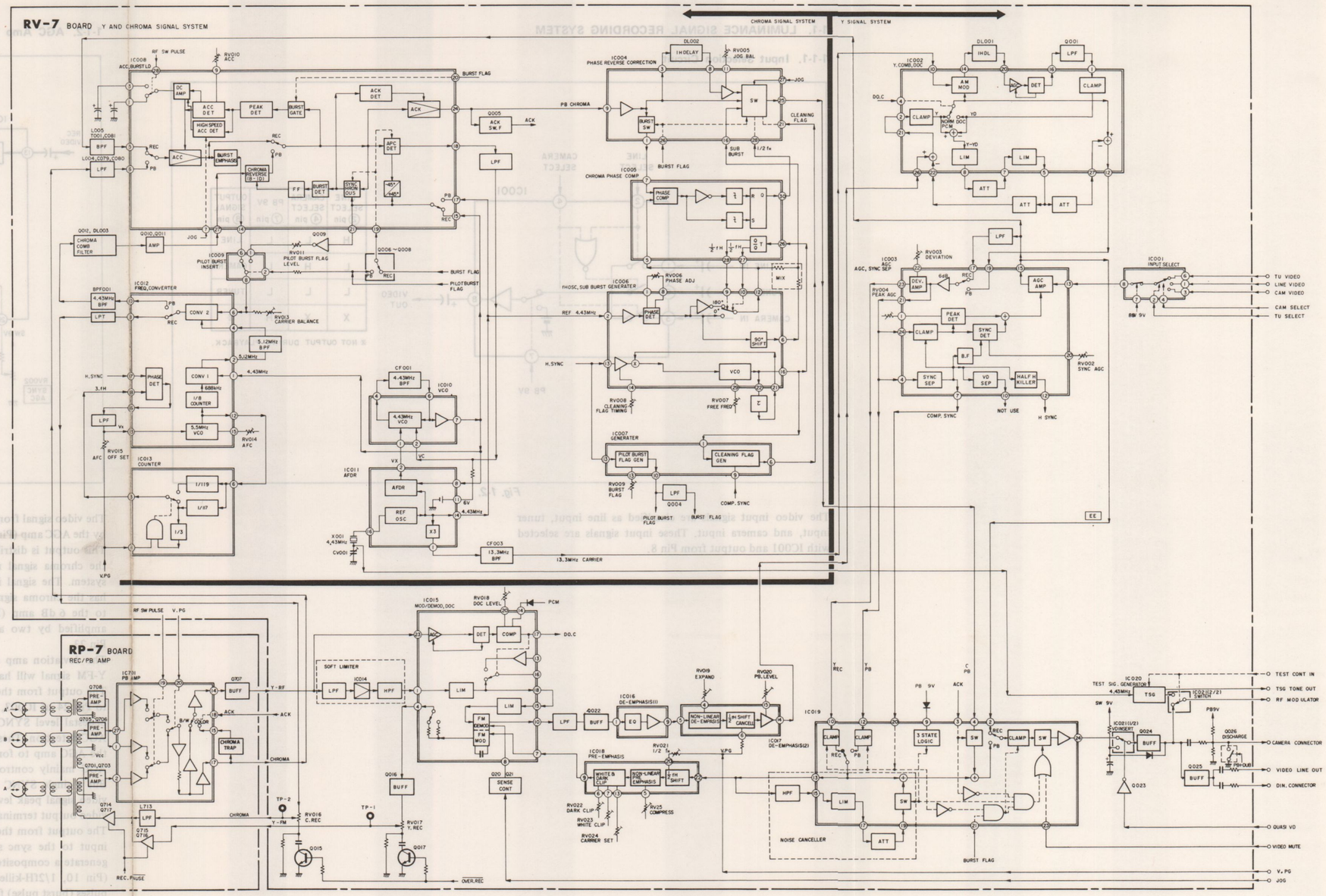
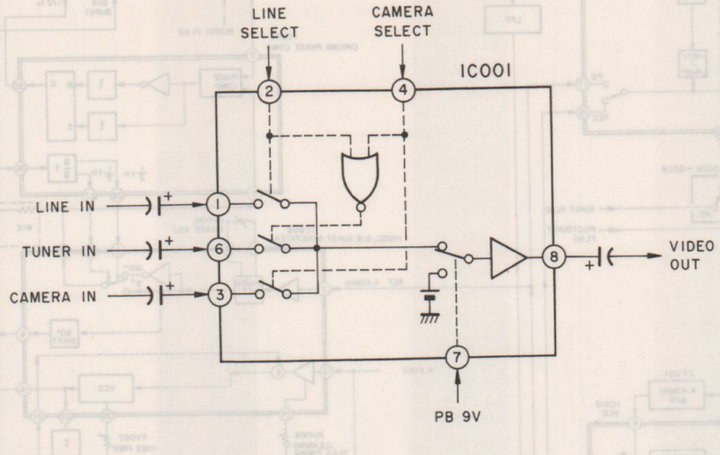


Fig. 1-1. Video System Block Diagram

1-1. LUMINANCE SIGNAL RECORDING SYSTEM

1-1-1. Input Selection Circuit



LINE SELECT ② pin	CAMERA SELECT ④ pin	PB 9V ⑦ pin	OUTPUT SIGNAL ⑧ pin
H	L	L	LINE
L	H	L	CAMERA
L	L	L	TUNER
X	X	H	※

※ NOT OUTPUT DURING PLAYBACK.

Fig. 1-2.

The video input signals are classified as line input, tuner input, and camera input. These input signals are selected with IC001 and output from Pin 8.

1-1-2. AGC Amp

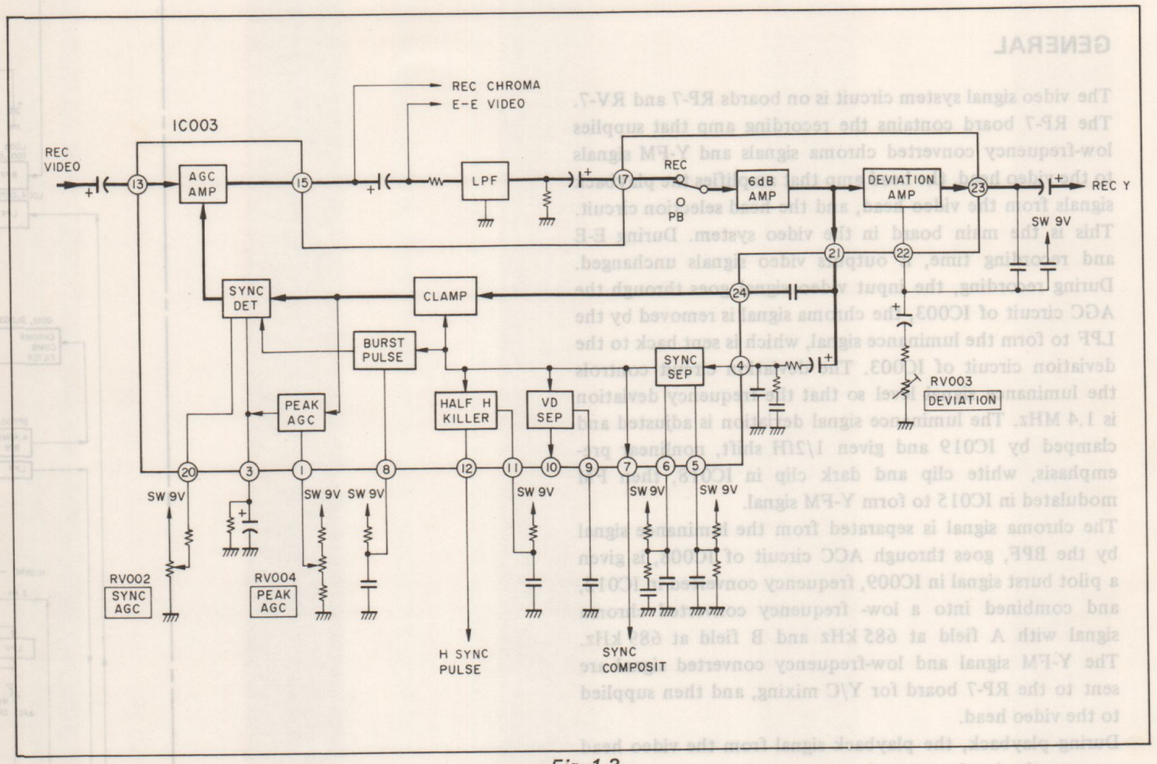


Fig. 1-3.

The video signal from input selection IC001 is level adjusted by the AGC amp (Pin 13 of IC003) and output from Pin 15. This output is distributed to the Y-signal recording system, the chroma signal recording system, and the E-E output system. The signal input to the Y-signal recording system has the chroma signal separated by the LPF and is input to the 6 dB amp (Pin 17 of IC003), where the signal is amplified by two and output, via the deviation amp, on Pin 23.

The deviation amp controls the Y-signal level so that the Y-FM signal will have a frequency deviation of 1.4 MHz. The output from the 6 dB amp (Pin 21 of IC003) is input to Pin 24 of IC003, and after sync tip clamping, undergoes pedestal level SYNC AGC detection and peak level PEAK AGC detection. These detection outputs are used to control the AGC amp to form an AGC loop. For AGC, the SYNC AGC mainly controls the sync signal to a constant level. But a single SYNC AGC may not be enough to keep the video signal peak level within the specified value (1 Vp-p at video output terminal). It is assisted by PEAK AGC.

The output from the 6 dB amp (Pin 21 of IC003) is further input to the sync separation circuit (Pin 4 of IC003) to generate a composite sync signal(Pin 7, vertical sync signal (Pin 10, 1/2fH-killed horizontal sync signal(Pin 12), and pulses (burst pulse) for SYNC AGC detection.

1-1-3. Pre-emphasis Circuit

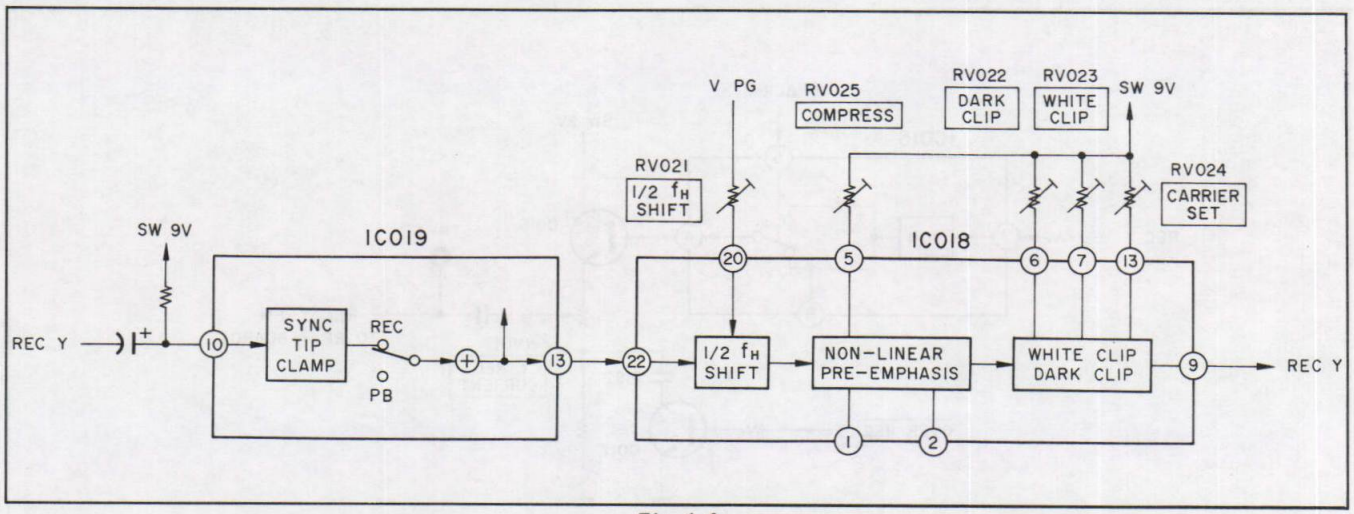


Fig. 1-4.

The output from the deviation amp is sync-tip clamped in IC019 and input to Pin 22 of IC018. IC018 shifts the carrier by 1/2fH, gives nonlinear pre-emphasis, white clip, and dark clip. The signal output is fed via Pin 9 to the FM modulator in IN015.

The 1/2fH carrier shift means that the difference in FM carrier frequencies recorded on adjacent tracks is 1/2fH (about 7.8 kHz), thereby allowing removal of crosstalk from adjacent tracks during playback by the use of the Y-signal comb filter. This is done by adding the V.PG signal (the same phase as RF SW pulse signal during recording), via RV021, to Pin 20 of IC018 so that the frequency difference in the FM carrier for A and B fields is controlled to 1/2fH. Nonlinear pre-emphasis improves the S/N ratio by varying the pre-emphasis characteristic and compressing the signal according to the signal input level (Fig. 1-5).

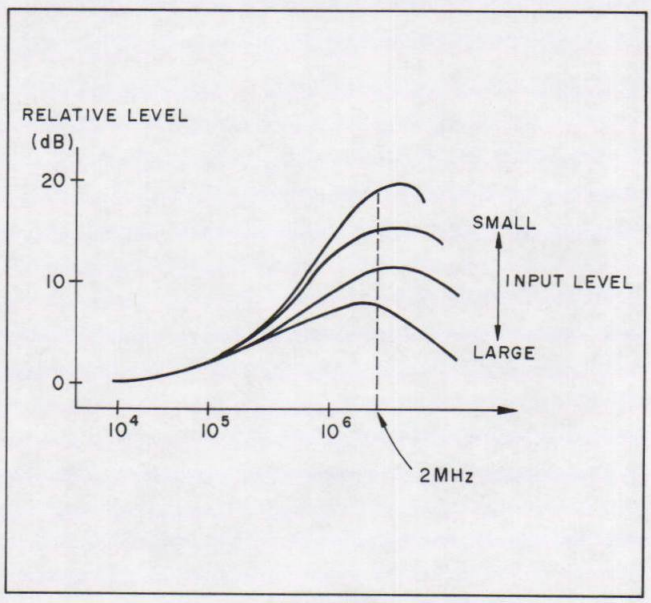


Fig. 1-5.

White clip and dark clip control the Y-signal generated by pre-emphasis so that the peak leading and trailing edges do not exceed the specified frequency deviation. The carrier is set so that the sync tip of Y-FM is at 3.8 MHz. In the SL-C9E, after adjusting the deviation, the sync-tip is clamped, then carrier adjustment follows; since these adjustments are independent of each other, alternate tracking is unnecessary.

1-1-4. FM Modulator

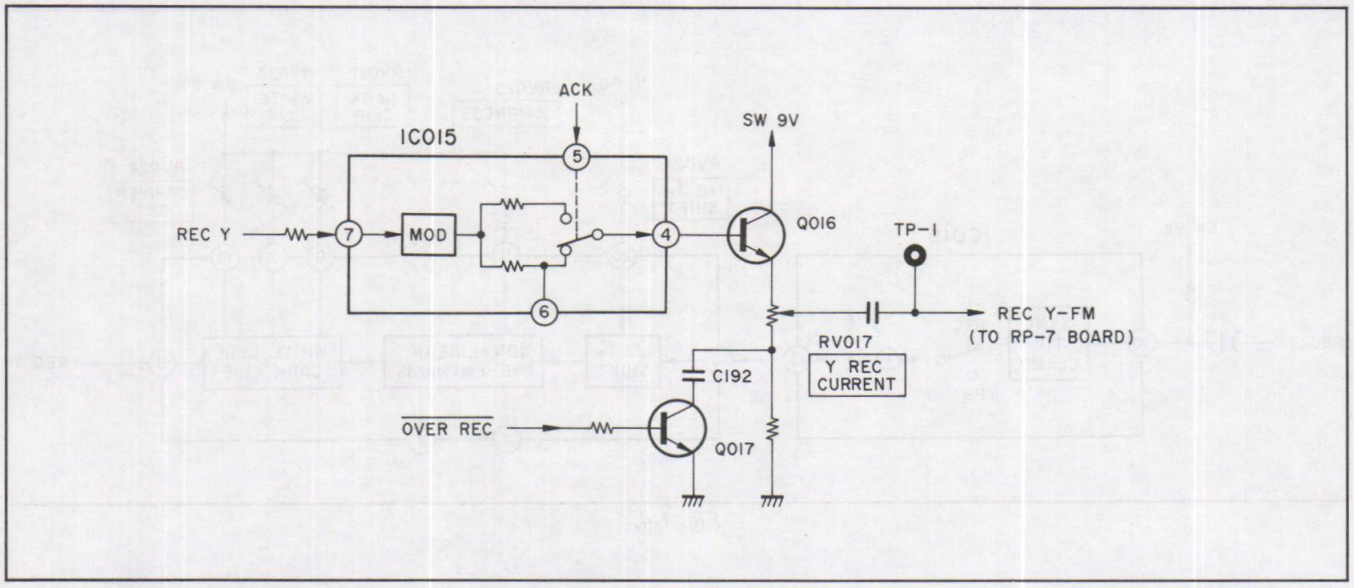


Fig. 1-6.

The output current from Pin 9 of IC018 is input to Pin 7 of IC015, the FM modulator, where it undergoes frequency modulation to form the Y-FM signal, and is output from Pin 4.

The output from Pin 4 of this frequency modulator is a square wave with frequency proportional to the current input on Pin 7.

The Y-FM signal goes via buffer Q016 to RV017 where recording current is adjusted, and is output to the RP-7 board. The ground of RV017 is connected to Q017. This transistor switch is ON in the REC mode, but turned OFF by OVER REC signal only during the over-record period at the beginning of recording. At this time, the recording current is about 20% bigger, so that recording is made while erasing the old record on the tape. C192 is used to prevent the video head being magnetized by transient variations in dc level due to Q017 turning on and off.

1-1-5. Recording Amp

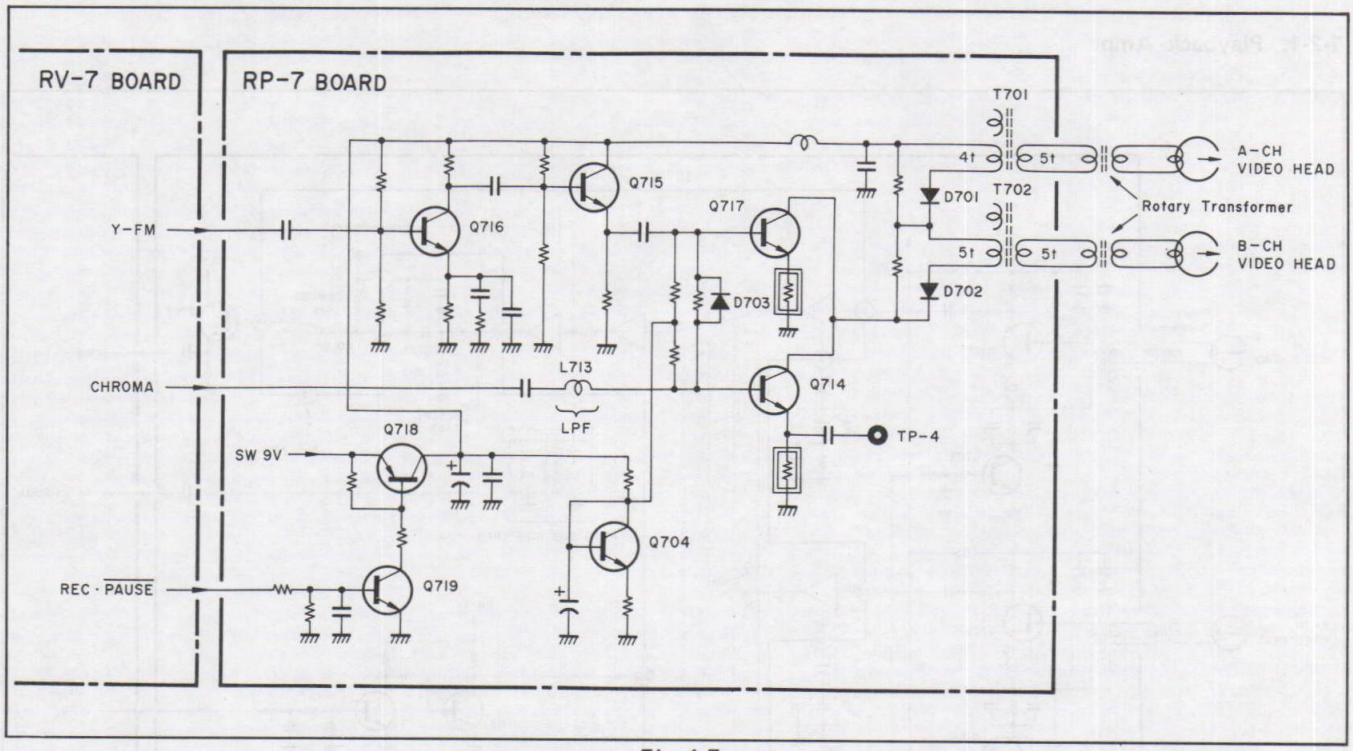


Fig. 1-7.

The Y-FM signal on the RP-7 board is amplified by Q716 and supplied via buffer Q175, to Q714 and Q717. At the same time, the low-frequency converted chroma signal is supplied, via low pass filter L713, to Q714 and superposed on the Y-FM signal. Q717 and Q714, connected in parallel, drive the tertiaries of record/playback transformers T701 and T702.

In the SL-C9E, the power voltage is 9V, less than the 12V of the earlier type (e.g. SL-C7E). This results in a lower transformer drive voltage (recording voltage). This drop in voltage is compensated by an increase in current. This is achieved by a decrease in impedance; the tertiaries of T701 and T702 have decreased number of windings, 4 turns for T701 and 5 turns for T702, as compared to 7.5 turns for the earlier type. The number of turns is greater in T702 (B-CH) than in T701 (A-CH); the reason is that the B-CH head, a composite head with A′-CH, must have recording current about 20% greater than that in A′-CH head.

The Y-FM signal is driven by both Q717 and Q714; this is to counteract the increased recording current. If a single transistor is used, distortion will be greater; and this is remedied by the additional use of Q714 originally for the chroma signal. At this time, Q717 receives the full Y-FM signal band, while Q714 receives the part that is left after the chroma band is removed by the low pass filter (L713). Therefore, the video head receives Y-FM recording current reduced by half in the chroma band.

Also, it leaves some Y-FM signal in the chroma band so that it will cancel any Y-signal that may leak into the chroma band during recording or playback. Because superposed chroma and Y-FM signals are input to Q714, the nonlinearity of Q714 causes beats. This is remedied by D703 that compensates for this nonlinearity. The emitter potentials for Q714 and Q717 are set low for efficient use of the power voltage. This may result in variations in collector current due to temperature change, and therefore Q704 is used as a temperature compensator to supply bias voltages to Q714 and Q717.

1-2. LUMINANCE SIGNAL REPRODUCTION SYSTEM

1-2-1. Playback Amp

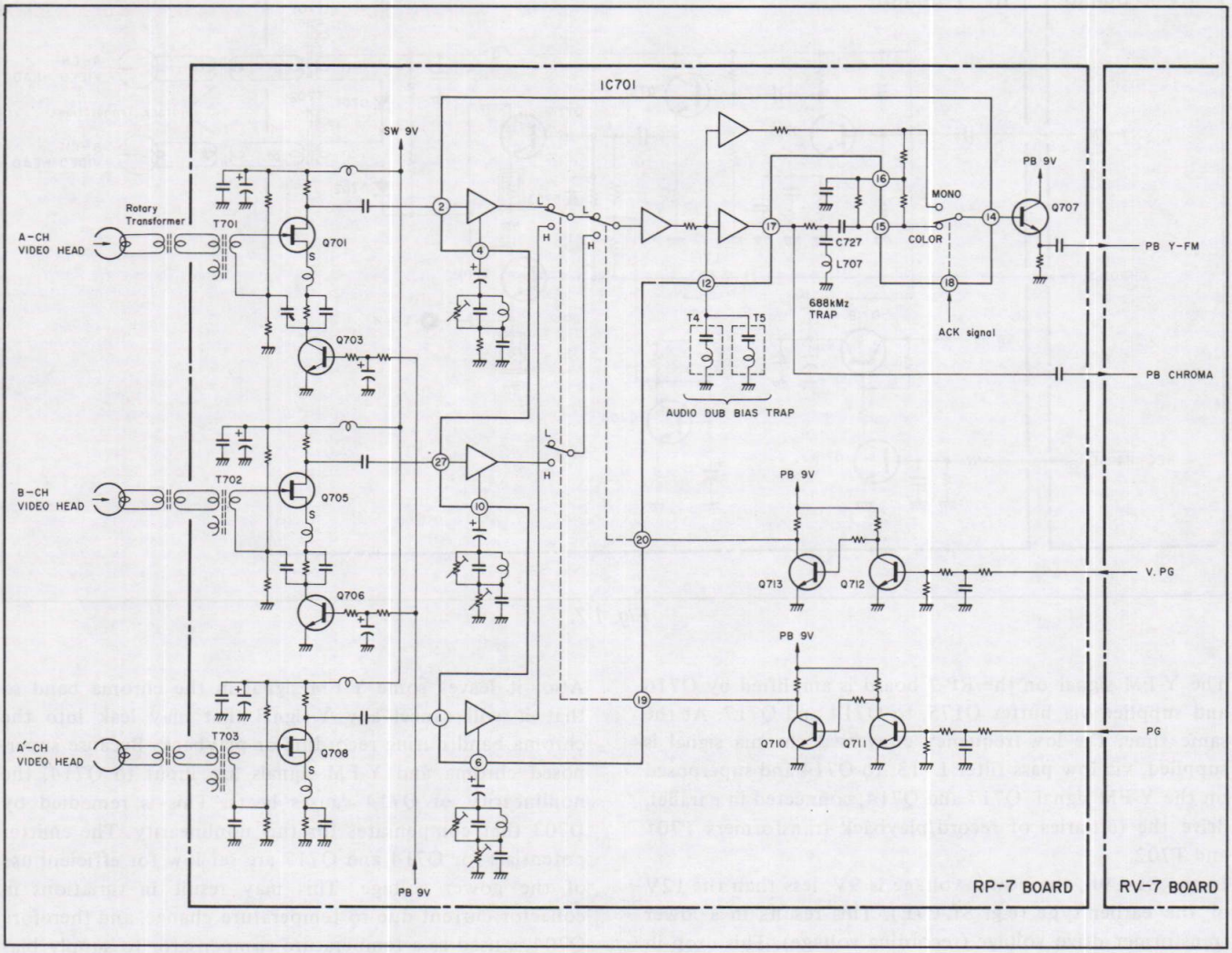


Fig. 1-8.

The RF signal reproduced in the A-CH head is fed to RP-7 board, stepped up by T701, and input to FET Q701. The signal is amplified in Q701 and input to Pin 2 of IC701. During playback, the record/playback select switch, Q703 is ON, and also Q701 is ON. During recording, Q703 is OFF, but Q701 does not operate. Q701 is reverse biased, and so does not affect the recording circuit.

From Pin 2 of IC701, the signal goes through the playback equalizer amp, and is input to the head selection circuit. The equalizer circuit enables low-frequency gain and high-frequency gain to be separately adjusted. This is also possible for B-CH. A'-CH is used exclusively for playback, and so has no record/playback selection circuit.

In normal playback mode, RF SW pulse and V.PG signals are in the same phase. When both signals are "L" and A-CH is "H", B-CH is selected.

During variable speed playback mode, the V.PG signal is "L" while the tape is stopped during slow playback, and when the RF SW pulse signal is "H", A'-CH head is selected instead of B-CH. In still and double speed playback modes, the V.PG signal is "L" all the time, and when the PF SW pulse is "H", A'-CH head is selected similarly. A'-CH head is not used in variable speed playback mode other than for the frame mode.

The RF signal output from the head selection circuit goes through the audio dubbing bias traps (T4 and T5) connected to Pin 12. Then, in the color mode, the signal is input to Pin 17, and via the chroma signal traps (688 kHz, L707 and C727), is output from Pin 14. In the black and white (B/W) mode, the signal is output, via IC from Pin 14.

This selection is done by the ACK DC signal input to Pin 18; color mode is selected when Pin 18 is "H"; B/W mode at "L". The Y-RF signal output from Pin 14 goes through buffer Q707 and is output to the RV-7 board. Buffer Q707 eliminates the effect of capacitance of the shield wires connecting the RP-7 and RV-7 boards.

The playback chroma signal is output to Pin 17. Q710 through Q713 eliminate noise from signals coming to the RP-7 board.

1-2-2. FM Demodulator and Dropout Detection

The Y-RF signal from the RP-7 board goes through the soft limiter circuit centering around IC014 and is input to Pin 1 of IC015. The signal is further limited in this IC and is output, via FM demodulator, from Pin 10. The demodulator sensitivity is controlled by Q20 and Q21. During variable speed playback, the sensitivity is raised by the JOG signal to reduce noise that occurs when the video head is offset from the track. The output from Pin 10 is sent, via low-pass filter Q022, to the de-emphasis circuit.

The Y-RF signal is also input to Pin 23 of IC015. The signal is sent to the AGC circuit in IC, detected and rectified, and input to the comparator. The AGC circuit compensates for the difference in Y-RF signal levels caused by the difference in tape sensitivity. In the comparator, the signal is compared with the reference voltage at Pin 20 to detect dropout, then the DOC pulse is output from Pin 17. The DOC pulse is sent to the Y comb filter (IC002) where the dropped-out Y-signal is compensated by the pre-1H Y-signal. The JOG signal is fed via D020 to Pin 14 of IC015 and via D018 to the PCM switch. During variable speed playback or PCM playback, this makes Pin 14 "H" and inhibits DOC circuit operation.

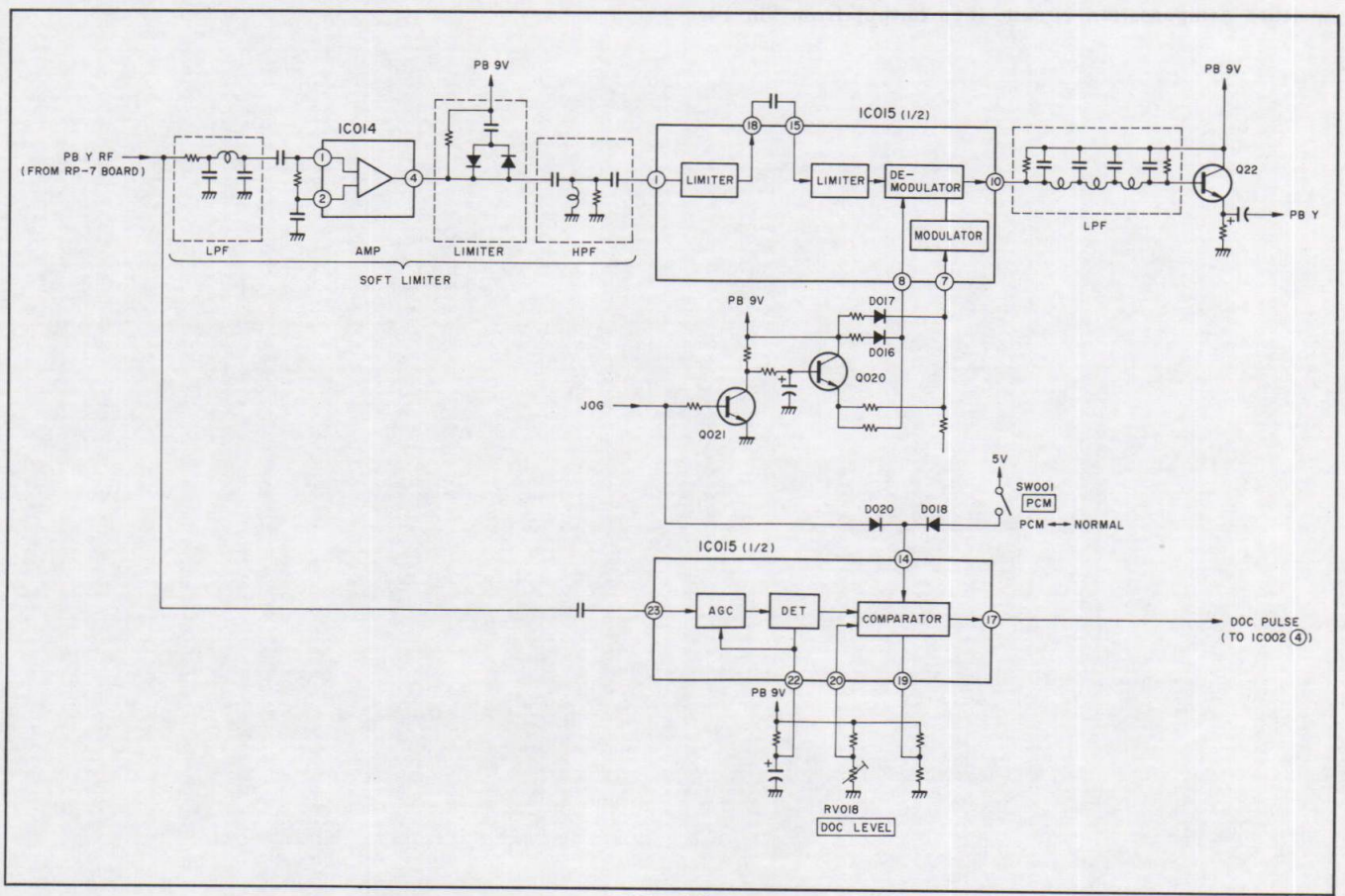


Fig. 1-9.

1-2-3. De-emphasis Circuit

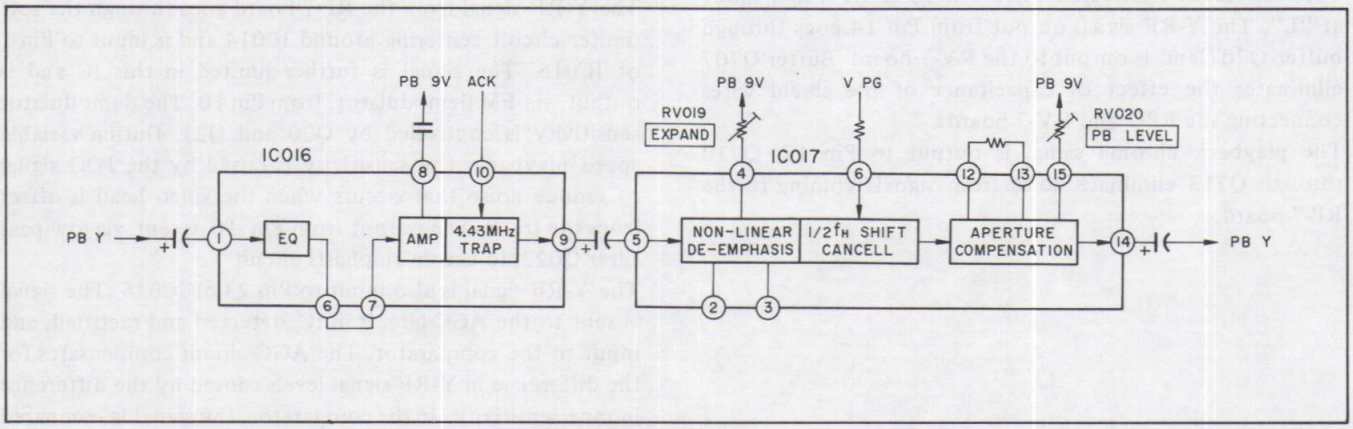


Fig. 1-10.

The FM demodulated Y-signal is fed via a low pass filter to Pin 1 of IC016, the equalizer circuit, that compensates for phase distortion caused by the low pass filter.
The Y-signal is amplified and the chroma band is separated in the 4.43 MHz trap. This trap is operated by the ACK signal from Pin 10 only in the color mode. The signal input to Pin 5 of IC017 is de-emphasised, expanded, and shifted back by 1/2fH, and high-frequency compensated by the aperture compensation circuit, then output from Pin 14.

1-2-4. Y-comb Filter

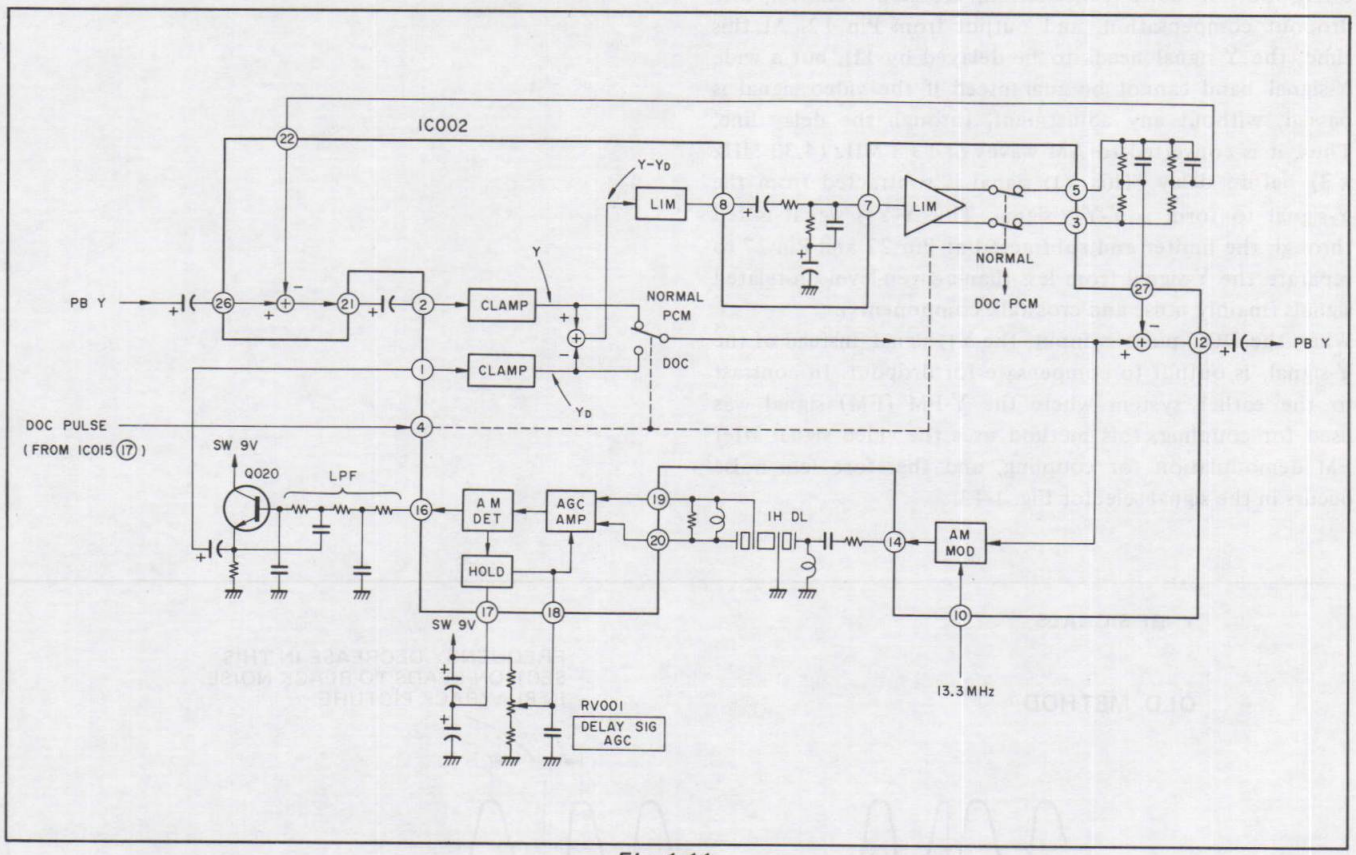


Fig. 1-11.

IC002 uses a 1H delay circuit to construct a Y-comb filter and dropout compensation circuit. The Y-comb filter uses 1H luminance signal linear corelation to remove noise not related to the line and crosstalk from the adjacent track. In recording a 1/2fH shift causes crosstalk from the adjacent track to be playbacked shifted by 1/2fH from the main signal, and thus the crosstalk can be removed by the comb filter. The comb filter as it is reduces the vertical resolution to half, and therefore operation is inhibited when the corelation signal(Y-YD) exceeds a given level Fig. 1-12.

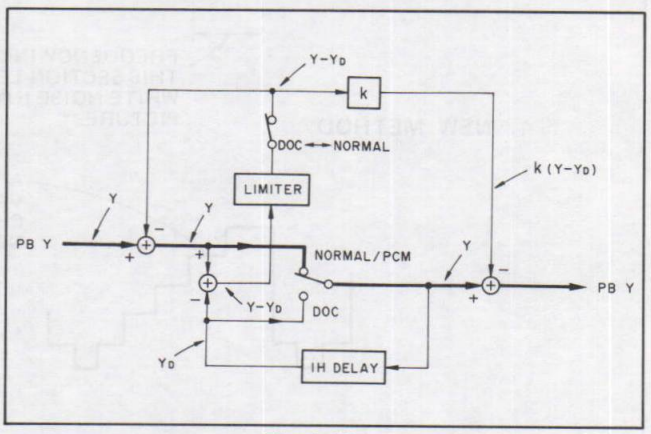


Fig. 1-12.

The Y-signal from the de-emphasis circuit is input to Pin 26 of IC002 for noise cancellation, crosstalk removal, and dropout compensation, and output from Pin 12. At this time, the Y-signal needs to be delayed by 1H, but a wide Y-signal band cannot be guaranteed if the video signal is passed, without any adjustment, through the delay line. Thus, it is converted to AM waves of 13.3 MHz (4.33 MHz x 3) before delay. This Y_D signal is subtracted from the Y-signal to form a Y-Y_D signal. This Y-Y_D signal is fed through the limiter and subtracted at Pin 22 and Pin 27 to separate the Y-signal from less-than-a-given-level un-related signals (mainly noise and crosstalk components).
When the DOC pulse is input, the Y_D signal, instead of the Y-signal, is output to compensate for dropout. In contrast to the earlier system where the Y-FM (FM) signal was used for coupling, this method uses the video signal after FM demodulation for coupling, and therefore less noise occurs in the signal selector Fig. 1-13.

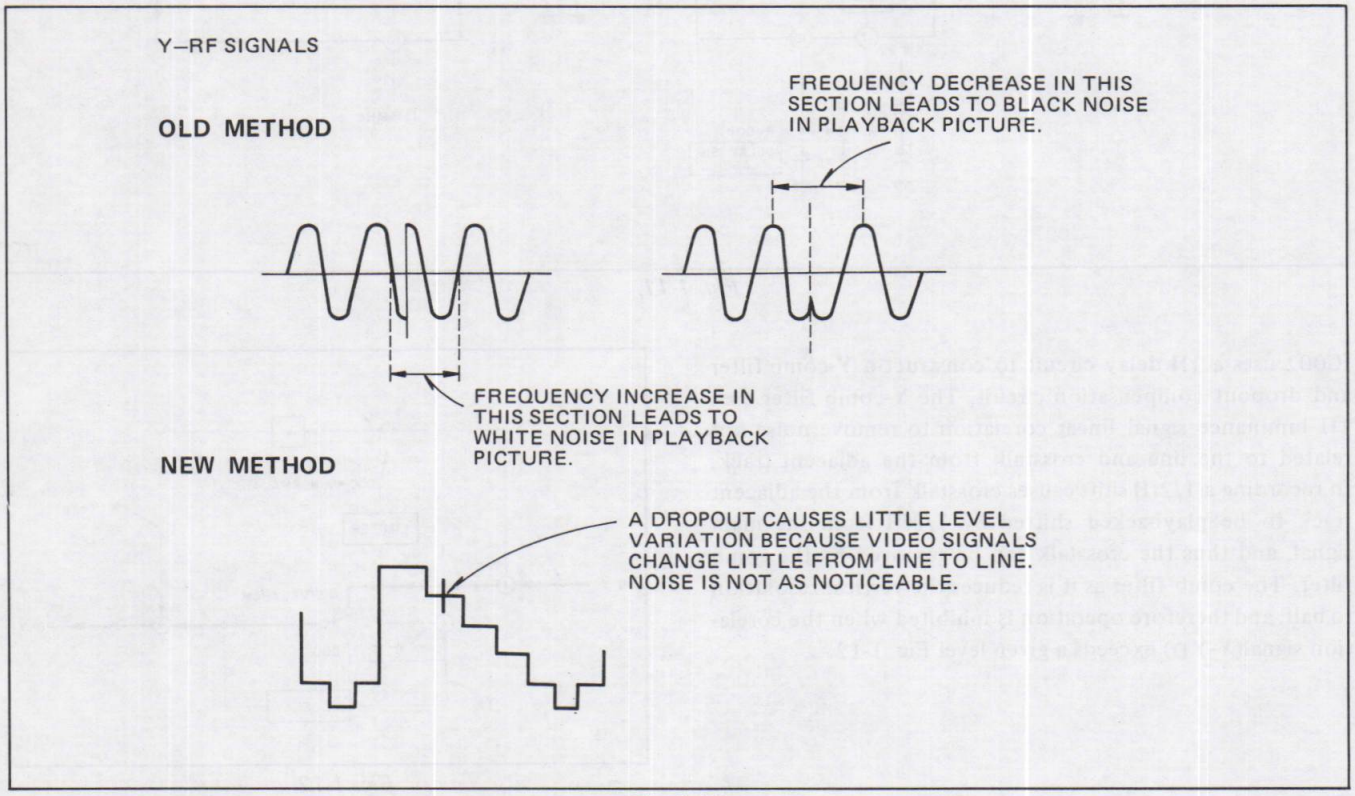


Fig. 1-13

1-2-5. 6-dB Amp and Sync Separation Circuit

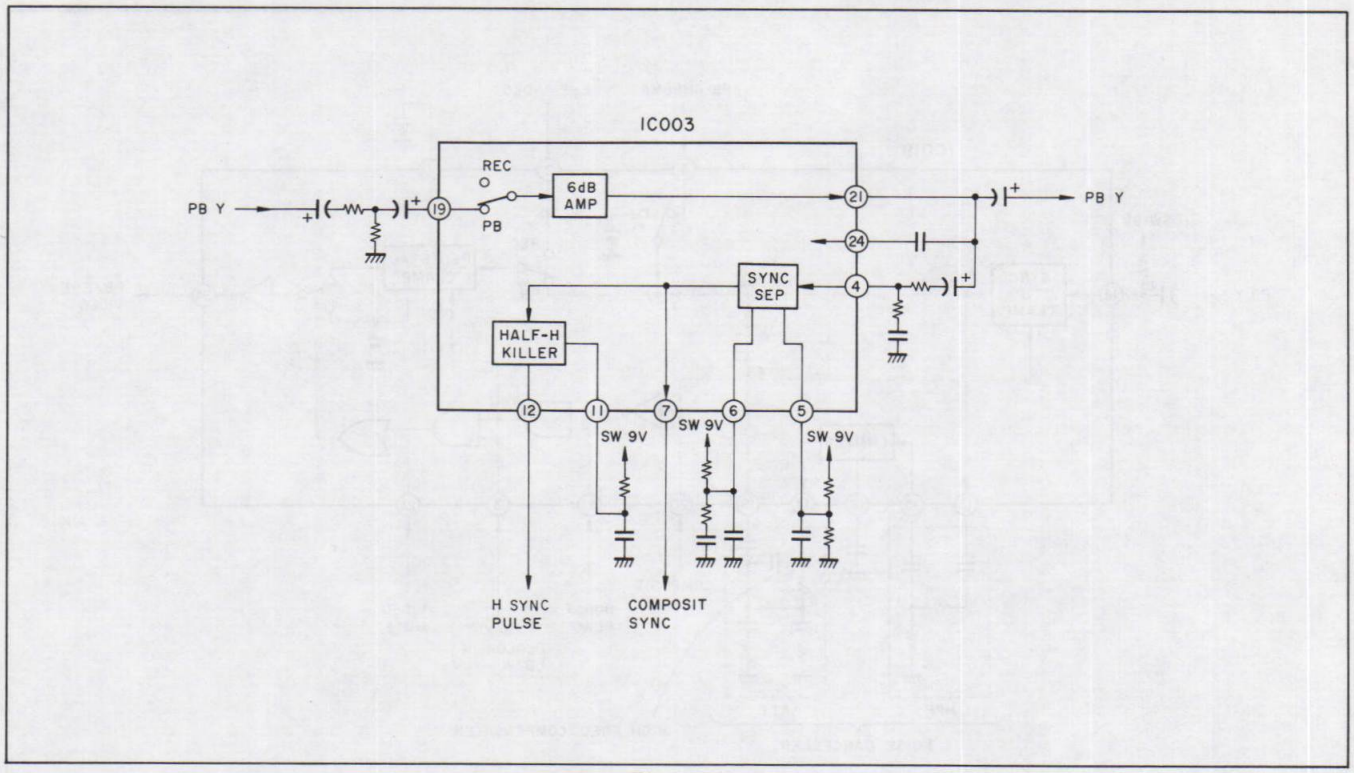


Fig. 1-14.

The output from the Y-comb filter is input to Pin 19 of IC003, times-two amplified, and output from Pin 21. In IC003, sync is separated and a composite sync signal and 1/2fH-killed horizontal sync signal are output. During playback, the AGC circuit is not used.

1-2-6. Noise Canceller and Y/C Mixer Circuit

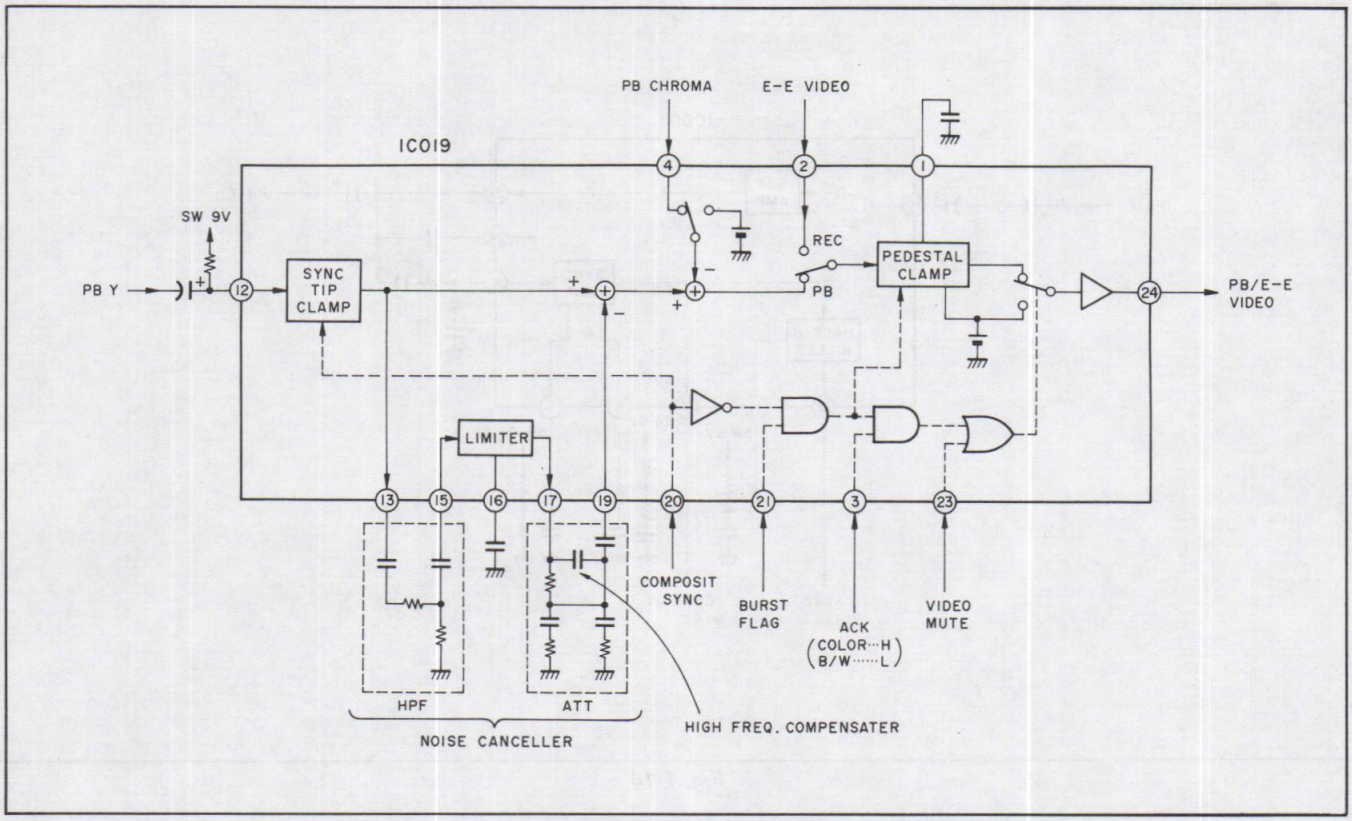


Fig. 1-15.

The output from IC003 is input to Pin 12 of IC019. This Y-signal is sync-tip clamped, goes through the noise canceller circuit, is mixed with the chroma signal input from Pin 4, to complete the video signal.

The noise canceller uses a high-pass filter and limiter to remove the high-frequency components from the Y-signal. This signal, being nearly all noise components, is subtracted from the original Y-signal to effectively remove the noise. The completed video signal is fed to a switch that selects it from the E-E video signal input to Pin 2, then input to both the pedestal clamp circuit and burst trap circuit. The burst trap operates so that, when the ACK signal on Pin 3 is "L", the video signal's burst period is replaced with the pedestal level by the use of a burst flag input on Pin 21. While the VTR's ACK signal is "L", the TV camera side VTR output monitor is in black and white (B/W) mode. The signal from the burst trap circuit, is fed from Pin 24 to the output circuit.

1-2-7. Output Circuit and Quasi-VD Insertion Circuit

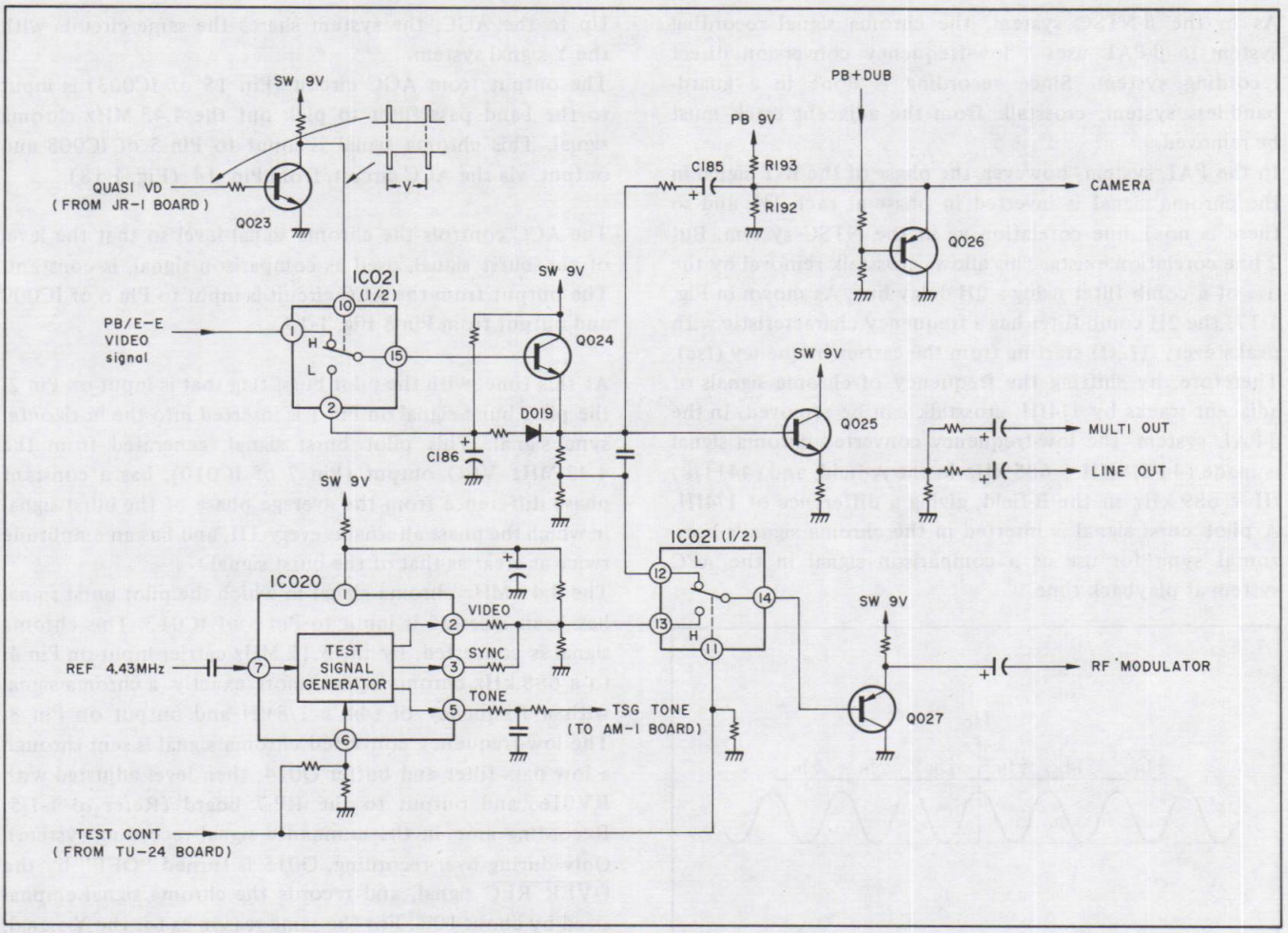


Fig. 1-16.

The video signal output from IC019 is input to Pin 1 of IC021. Pin 10 of this IC is normally "H", so that the input to Pin 1 is output from Pin 15 without change. During variable speed playback, however, the Quasi-VD signal output from the slow servo circuit on the JR-1 board causes the voltage at Pin 10 to go "L" during the period of quasi-VD insertion. At this time, D019 and C186 maintain the potential on Pin 2 at the video signal sync-tip level, and as a result, Pin 15 outputs a video signal in which a quasi-vertical sync signal is inserted. The output from Pin 15 of IC021, after passing through buffer Q024, is divided into three.

The first is output, via C185, to the camera connector. During playback, R193 and R192 select the VTR output for the monitor screen at the camera side by superposing a dc voltage on the video signal. At the moment the playback mode is switched to another mode, Q026 is turned ON and discharges camera-side input capacitor and speeds up the switching speed of the camera monitor.

The second is the line output via buffer Q025.

The third is output, via IC021 and buffer Q027, to the RF modulator. When the test signal switch is ON, this IC021 switches the RF modulator output to a test signal.

1-3. CHROMA SIGNAL SYSTEM

As in the β-NTSC system, the chroma signal recording system in β-PAL uses a low-frequency conversion direct recording system. Since recording is done in a guard-band-less system, crosstalk from the adjacent track must be removed.

In the PAL system, however, the phase of the R-Y signal in the chroma signal is inverted in phase at each 1H, and so there is no 1 line corelation as in the NTSC system. But 2 line corelation exists. This allows crosstalk removal by the use of a comb filter using a 2H delay line. As shown in Fig. 1-17, the 2H comb filter has a frequency characteristic with peaks every 1/2fH starting from the carrier frequency (fsc). Therefore, by shifting the frequency of chroma signals of adjacent tracks by 1/4fH, crosstalk can be removed. In the β-PAL system, the low-frequency converted chroma signal is made (44-1/8)fH ≒ 685 kHz in the A-field, and (44+1/8) fH ≒ 689 kHz in the B-field, giving a difference of 1/4fH. A pilot burst signal is inserted in the chroma signal's horizontal sync for use as a comparison signal in the APC system at playback time.

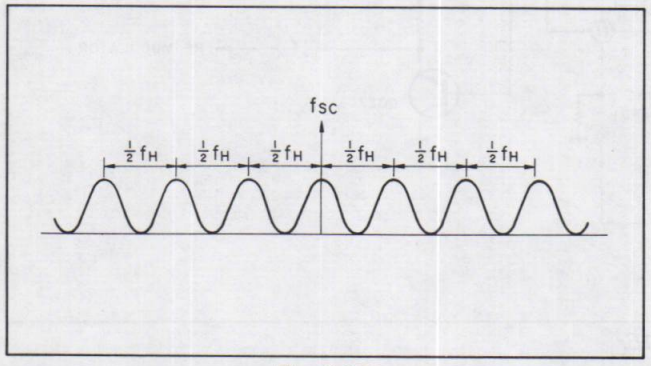


Fig. 1-17.

1-3-1. Chroma Signal Recording System

Up to the AGC, the system shares the same circuits with the Y-signal system.

The output from AGC circuit (Pin 15 of IC003) is input to the band pass filter to pick out the 4.43 MHz chroma signal. This chroma signal is input to Pin 5 of IC008 and output, via the ACC circuit, from Pin 14 (Fig. 1-18).

The ACC controls the chroma signal level so that the level of the burst signal, used as comparison signal, is constant. The output from the ACC circuit is input to Pin 6 of IC009 and output from Pin 8 Fig. 1-19.

At this time, with the pilot burst flag that is input on Pin 2, the pilot burst signal on Pin 1 is inserted into the horizontal sync signal. This pilot burst signal, generated from the 4.43 MHz VCO output (Pin 7 of IC010), has a constant phase difference from the average phase of the burst signal in which the phase alternates every 1H, and has an amplitude twice as great as that of the burst signal.

The 4.43 MHz chroma signal in which the pilot burst signal has been inserted is input to Pin 6 of IC012. This chroma signal is converted, by the 5.12 MHz carrier input on Pin 4, to a 688 kHz chroma signal (more exactly, a chroma signal with a frequency of (44 ± 1/8)fH and output on Pin 8. The low-frequency converted chroma signal is sent through a low pass filter and buffer Q014, then level adjusted with RV016, and output to the RP-7 board (Refer to 1-1-5, Recording amp in the luminance signal recording system). Only during over-recording, Q015 is turned "OFF" by the $\overline{\text{OVER REC}}$ signal, and records the chroma signal emphasized by about 10%. For the same reason as for the Y-signal, C191 is inserted to prevent magnetization of video heads.

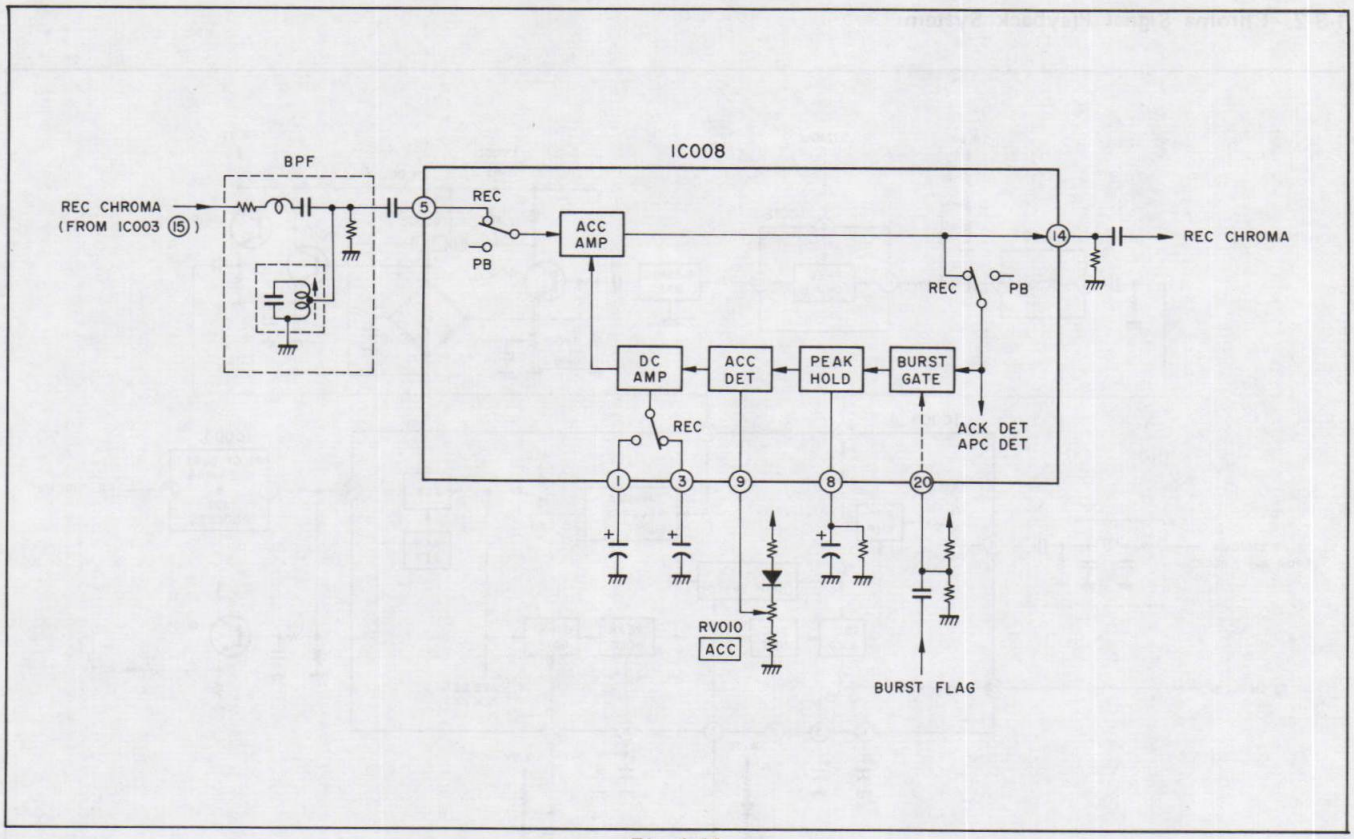


Fig. 1-18.

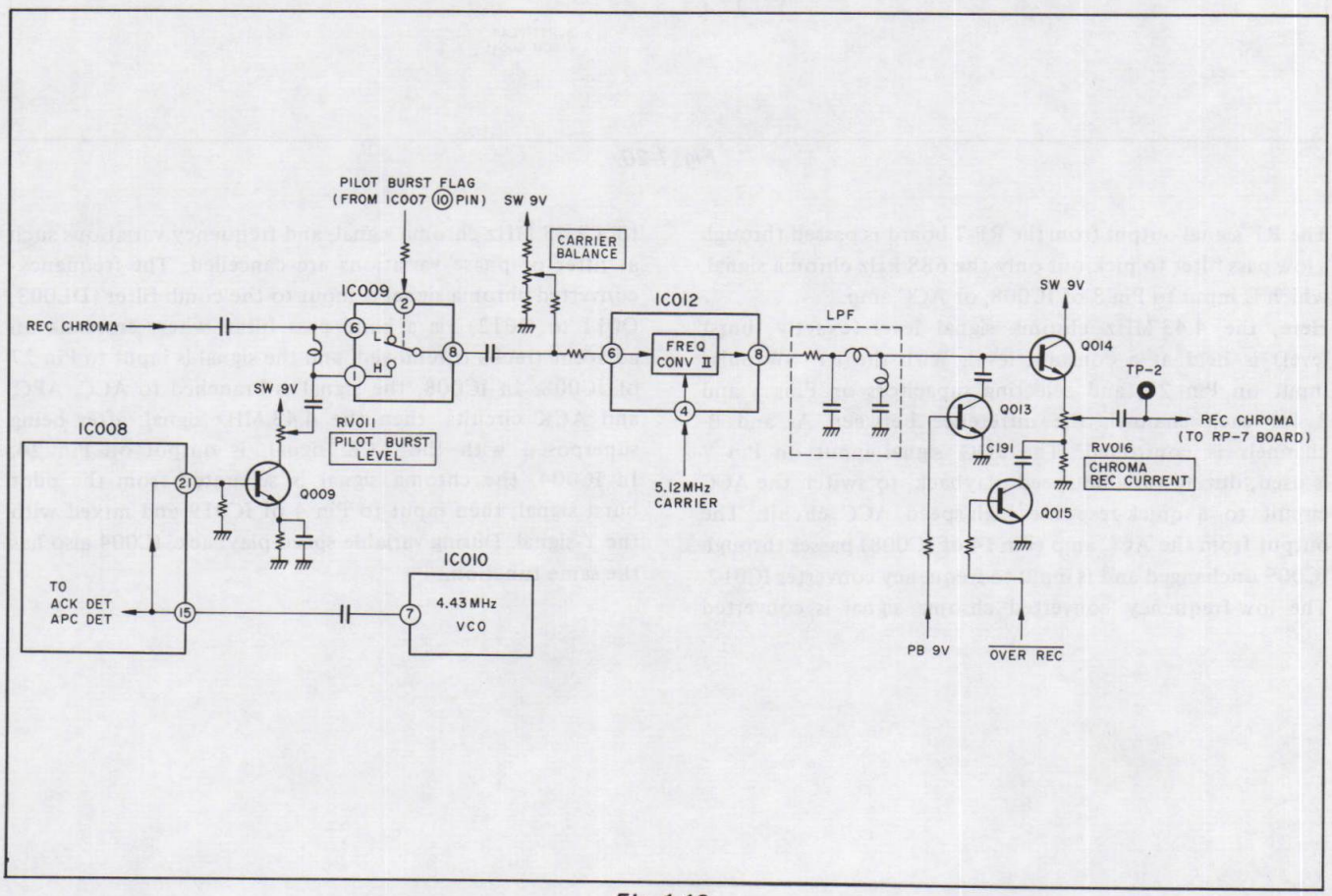


Fig. 1-19.

1-3-2. Chroma Signal Playback System

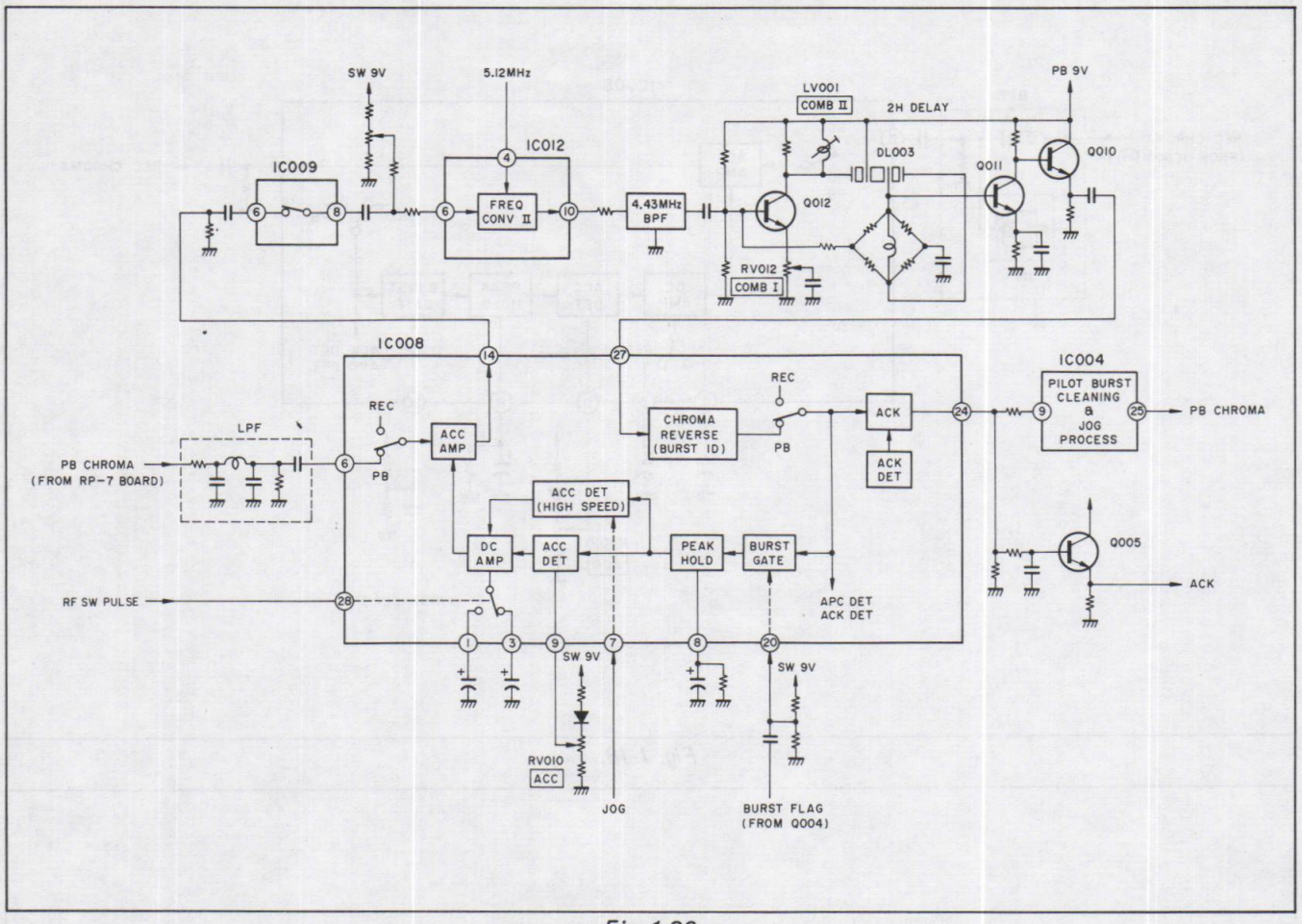


Fig. 1-20.

The RF signal output from the RP-7 board is passed through a low pass filter to pick out only the 688 kHz chroma signal, which is input to Pin 8 of IC008, or ACC amp.

Here, the 4.43 MHz chroma signal level (exactly, burst level) is held at a constant level. With the RF SW pulse input on Pin 28, and selecting capacitors on Pins 1 and 3 for each channel, the difference between A- and B-channels is controlled. The JOG signal input on Pin 7 is used, during variable speed playback, to switch the ACC circuit to a quick-response high-speed ACC circuit. The output from the ACC amp (Pin 14 of IC008) passes through IC009 unchanged and is input to frequency converter IC012. The low-frequency converted chroma signal is converted to a 4.43 MHz chroma signal, and frequency variations such as jitter or phase variations are cancelled. The frequency-converted chroma signal is input to the comb filter (DL003, Q011 to Q012) via a band pass filter, where crosstalk on adjacent tracks is removed, and the signal is input to Pin 27 of IC008. In IC008, the signal is branched to ACC, APC, and ACK circuits, then the 4.43 MHz signal, after being superposed with the ACK signal, is output on Pin 24. In IC004, the chroma signal is separated from the pilot burst signal, then input to Pin 4 of IC019 and mixed with the Y-signal. During variable speed playback, IC004 also has the same function.

1-3-3. Frequency Conversion Circuit

Frequency conversion is carried out in IC012. The 688 kHz output from the AFC circuit and the 4.43 MHz output from the APC circuit are input to the first frequency converter to generate a 5.12 MHz signal. This signal is added to the second frequency converter. In recording, this operation is used to convert the 4.43 MHz chroma signal to a 688 kHz chroma signal; in playback, the 688 kHz signal is converted to a 4.43 MHz chroma signal (Figs. 1-21 and 22).

1) IN RECORDING

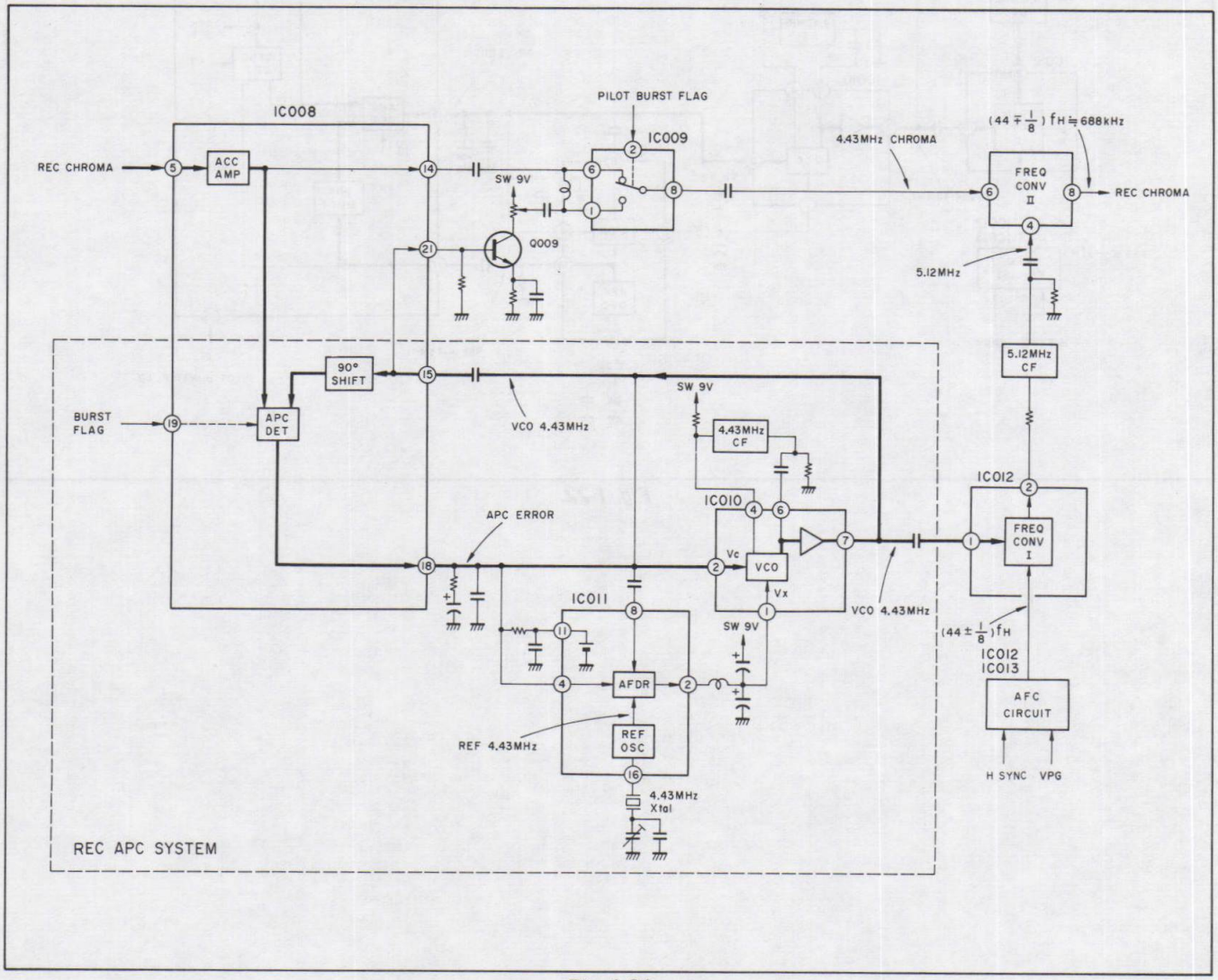


Fig. 1-21.

2) DURING PLAYBACK

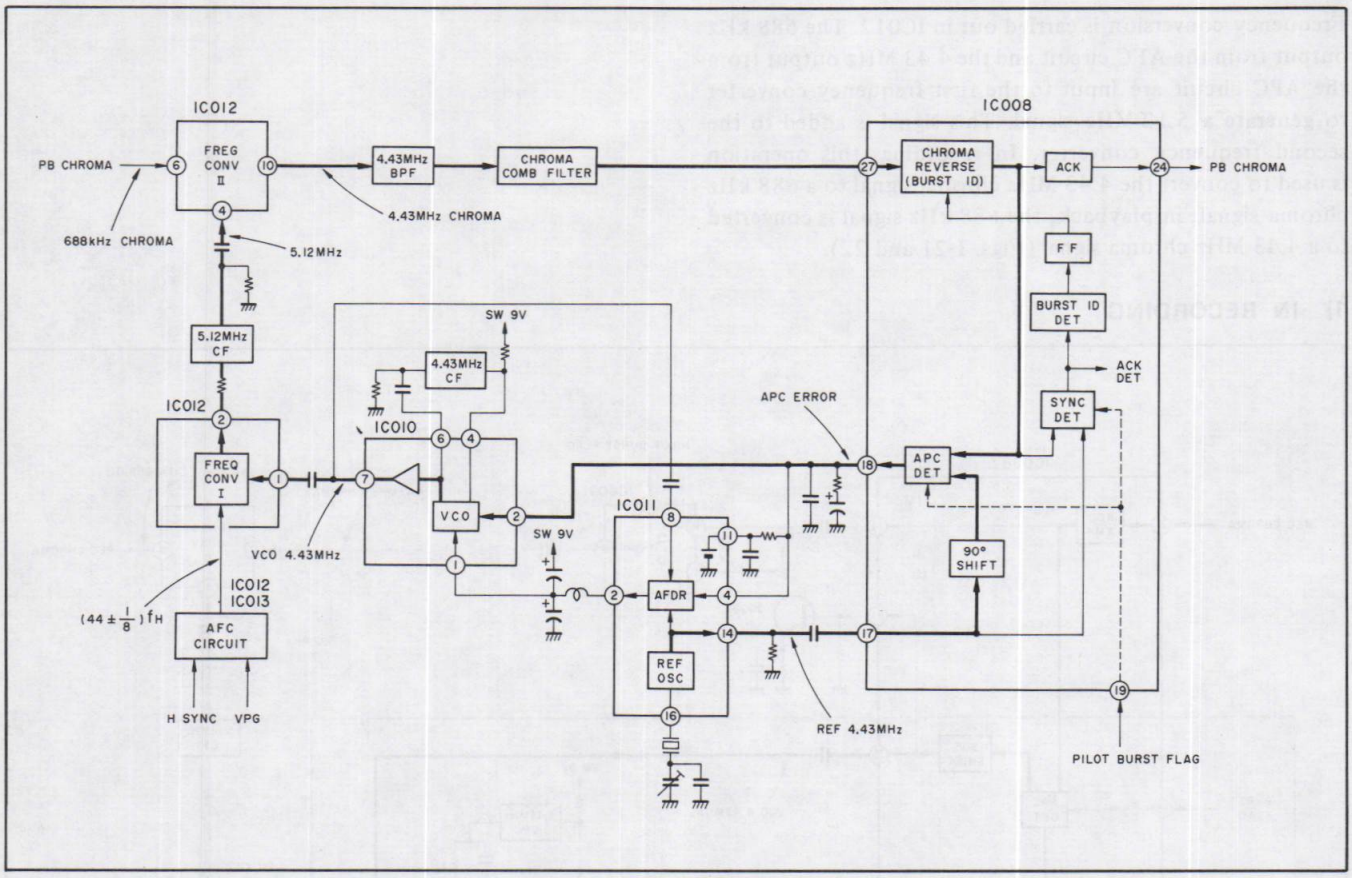


Fig. 1-22.

1-3-4. AFC Circuit

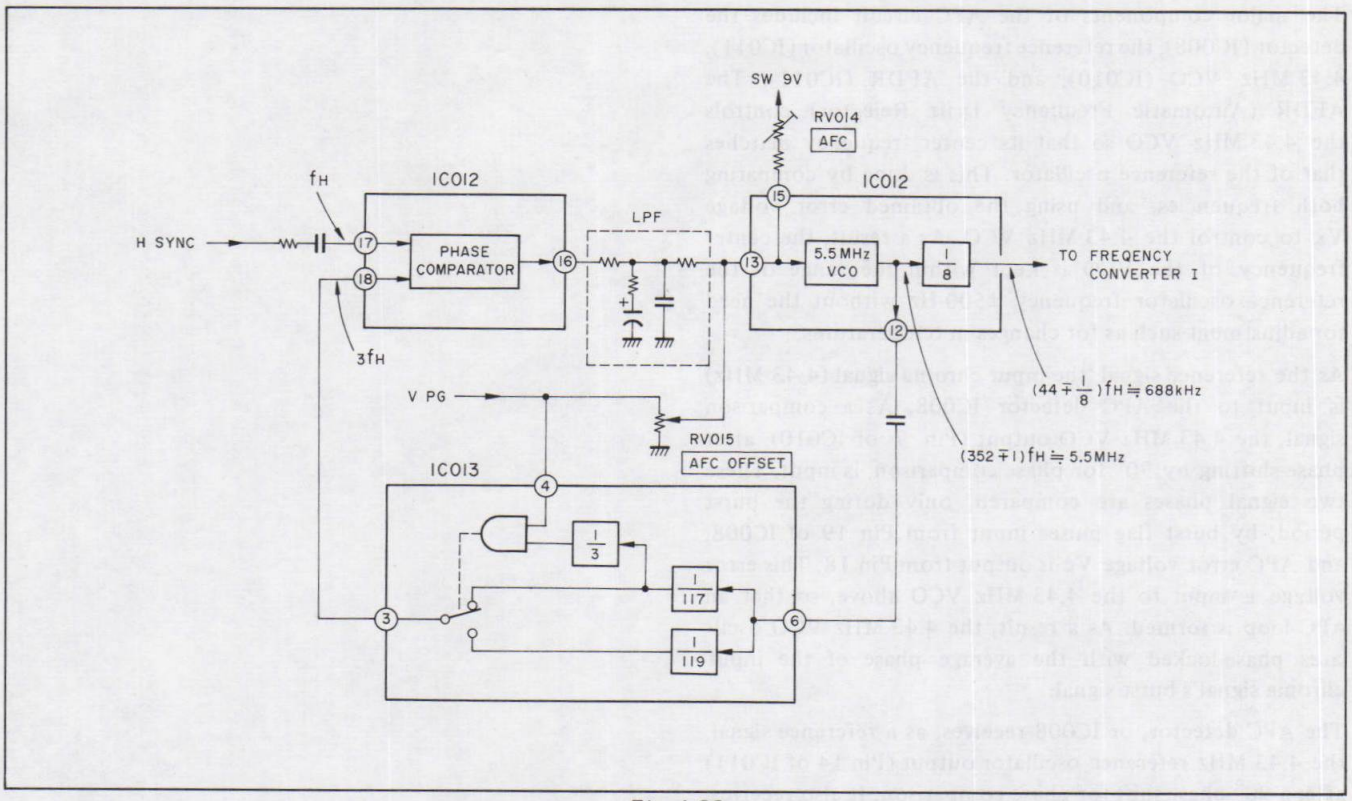


Fig. 1-23.

This circuit comprises IC012 and IC013. The 5.5 MHz VCO output from Pin 12 of IC012 is input to Pin 6 of IC013. When the V.PG signal on Pin 4 is "L" (A-field), IC013 counts down the input on Pin 6 to 1/117 and outputs it on Pin 3. When "H" (B field), by combining 1/117 and 1/119 in a time ratio of 1:2, the input is count down to 1/117.666 and output on Pin 3. This output from Pin 3 of IC013 is about 47 kHz (3fH). This is input to Pin 18 of IC012 to compare its phase with that of the horizontal sync signal that was input to Pin 17; and this error voltage is used to control the 5.5 MHz VCO. This causes the output frequency from Pin 3 of IC013 to be locked with the horizontal sync signal, giving 3fH. As a result, the 5.5 MHz VCO oscillates, in the A field, at a frequency of fH x 3 x 117 = 351 fH, and in the B field, at fH x 3 x 117.666 ≒ 353fH.

In IC012, this VCO output is count down to 1/8 and input to the first frequency converter. The frequency is given (44 ± 1/8) fH, or about 688 kHz.

In the earlier AFC circuit, the signal count down to fH is compared with the horizontal sync signal; in this circuit, a 3fH signal is used for comparison.

Comparison with 3fH makes the locking time smaller. The AFC functions are as follows:

1) IN RECORDING

Outputs a signal with the input-video-signal-synchronized frequency (44 ± 1/8)fH.

2) IN PLAYBACK

Variations in the relative speed of the video head and tape result in frequency variations in the playback signal. This must be corrected to reproduce the correct color. The AFC circuit cancels the frequency variations in the chroma signal. Assuming the frequency variations in the horizontal sync signal to be +Δf, the frequency variation in the playback chroma signal may be given by + (44 ± 1/8) x Δf.

Supposing that the horizontal sync signal frequency varies by +Δf, the variation in the output frequency (688 kHz) of the AFC circuit may be (44 ± 1/8) x Δf. This frequency variations will cause, in the first frequency conversion circuit output (5.12 MHz), frequency variations of + (44 ± 1/8)Δf.

This 5.12-MHz signal and playback chroma signal (688 kHz) are input to the second frequency converter, and the chroma signal with the differential frequency (4.43 MHz) is output. The frequency variations are both + (44 ± 1/8)Δf, and as a result, the frequency variations in this converter output are cancelled out.

1-3-5. APC Circuit

The major components of the APC circuit includes the detector (IC008), the reference frequency oscillator (IC011), 4.43 MHz VCO (IC010), and the AFDR (IC011). The AFDR (Automatic Frequency Drift Rejector) controls the 4.43 MHz VCO so that its center frequency matches that of the reference oscillator. This is done by comparing both frequencies, and using the obtained error voltage Vx to control the 4.43 MHz VCO. As a result, the center frequency of the VCO is kept within the range of the reference oscillator frequency ±500 Hz without the need for adjustment such as for changes in temperatures.

As the reference signal, the input chroma signal (4.43 MHz) is input to the APC detector IC008. As a comparison signal, the 4.43 MHz VCO output (Pin 7 of IC010), after phase-shifting by 90° for phase comparison, is input. These two signal phases are compared, only during the burst period, by burst flag pulses input from Pin 19 of IC008, and APC error voltage Vc is output from Pin 18. This error voltage is input to the 4.43 MHz VCO above, so that an APC loop is formed. As a result, the 4.43 MHz VCO oscillates phase-locked with the average phase of the input chroma signal's burst signal.

The APC detector, or IC008 receives, as a reference signal, the 4.43 MHz reference oscillator output (Pin 14 of IC011) after a 90° phase shift for phase comparison. It also receives, as a comparison signal, the playback chroma signal (4.43 MHz) after frequency conversion. These two signal phases are compared only during the pilot burst period, by pilot burst flag pulses input from Pin 19 of IC008, and APC error voltage Vc is output on Pin 18. This error voltage is input to the 4.43 MHz VCO and shifts its oscillation phase. This phase shift is transmitted, through the first and second frequency converters, to the playback chroma signal, and cancels the phase error between the pilot burst signal and the output signal from the reference oscillator.
The APC loop thus removes the phase variations in the playback chroma signal by causing the chroma signal pilot burst phase to be locked with the output signal from the reference oscillator. In this manner, the APC circuit removes phase variations that the AFC circuit is unable to remove. There is a burst ID circuit in the APC loop. Suppose that, at the beginning of playback, when selecting the head, or at dropout, the playback chroma signal is 180° out of phase with the reference oscillation. In this case, the APC circuit is unstable and the APC response time is longer. In such a case, playback chroma signal phase is inverted to shorten the APC circuit response time.

1-3-6. ACK Circuit

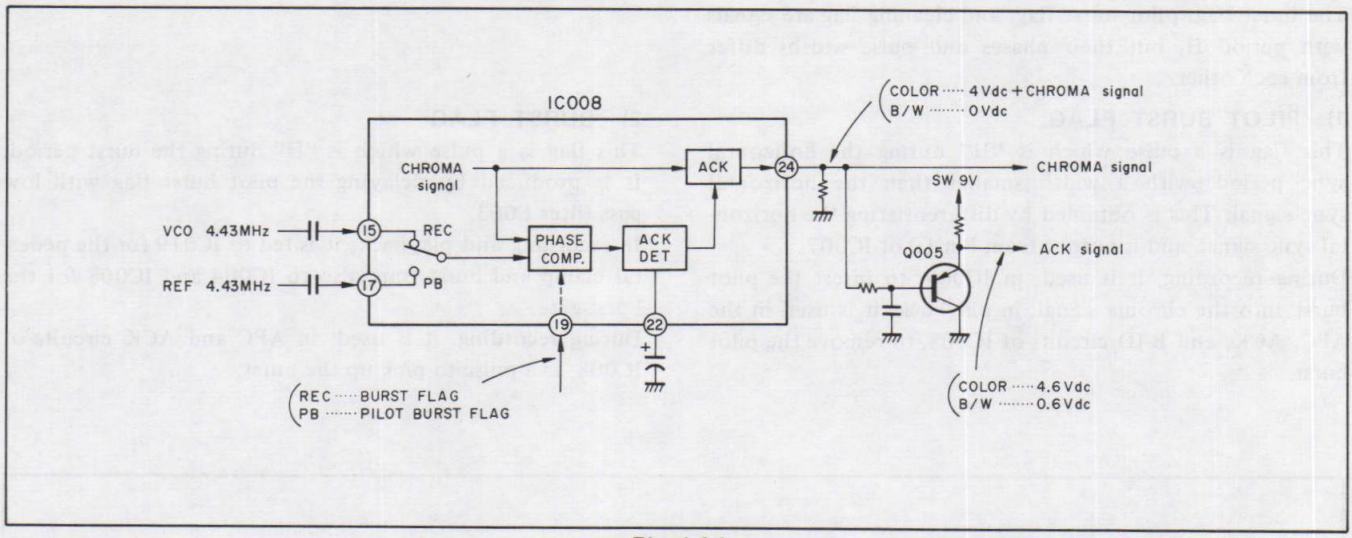


Fig. 1-24.

The ACK circuit is in IC008. Color or B/W mode is discriminated by sync detection with the burst signal during recording, and with the pilot burst signal, during playback. The reason is that the pulse input to Pin 19 is either the burst flag or pilot burst flag, depending on whether recording or playing back. The ACK signal is output from Pin 24 . Pin 24 also outputs the chroma signal.

In color mode, 4V dc and chroma signal are output; in B/W mode, the output is 0V dc. Thereafter, the ACK signal is separated from the chroma signal in the low pass filter Q005.

1-3-7. Burst Flag, Pilot Burst Flag and Cleaning Flag

The burst flag, pilot burst flag, and cleaning flag are signals with period H, but their phases and pulse widths differ from each other.

1) PILOT BURST FLAG

This flag is a pulse which is "H" during the horizontal sync period, with a width smaller than the horizontal sync signal. This is obtained by differentiating the horizontal sync signal, and is output from Pin 10 of IC007.

During recording, it is used, in IC009, to insert the pilot burst into the chroma signal; in playback, it is used in the APC, ACK, and B-ID circuits of IC008, to remove the pilot burst.

2) BURST FLAG

This flag is a pulse which is "H" during the burst period. It is produced by delaying the pilot burst flag with low pass filter L003.

In recording and playback, it is fed to IC019 for the pedestal clamp and burst trap, also to IC004 and IC008 for the burst gate.

During recording, it is used, in APC and ACK circuits of IC008, as a pulse to pick up the burst.

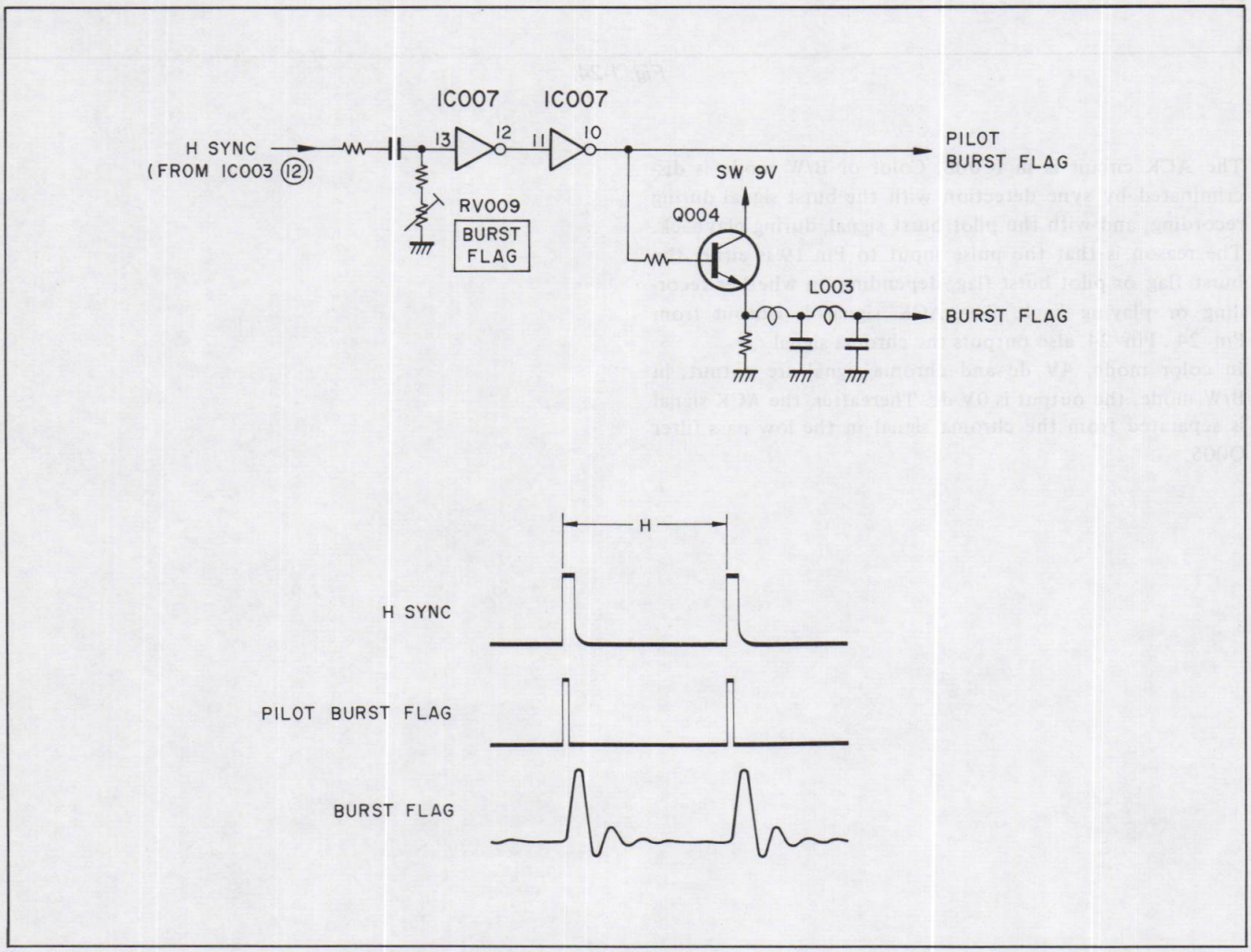


Fig. 1-25.

3) CLEANING FLAG

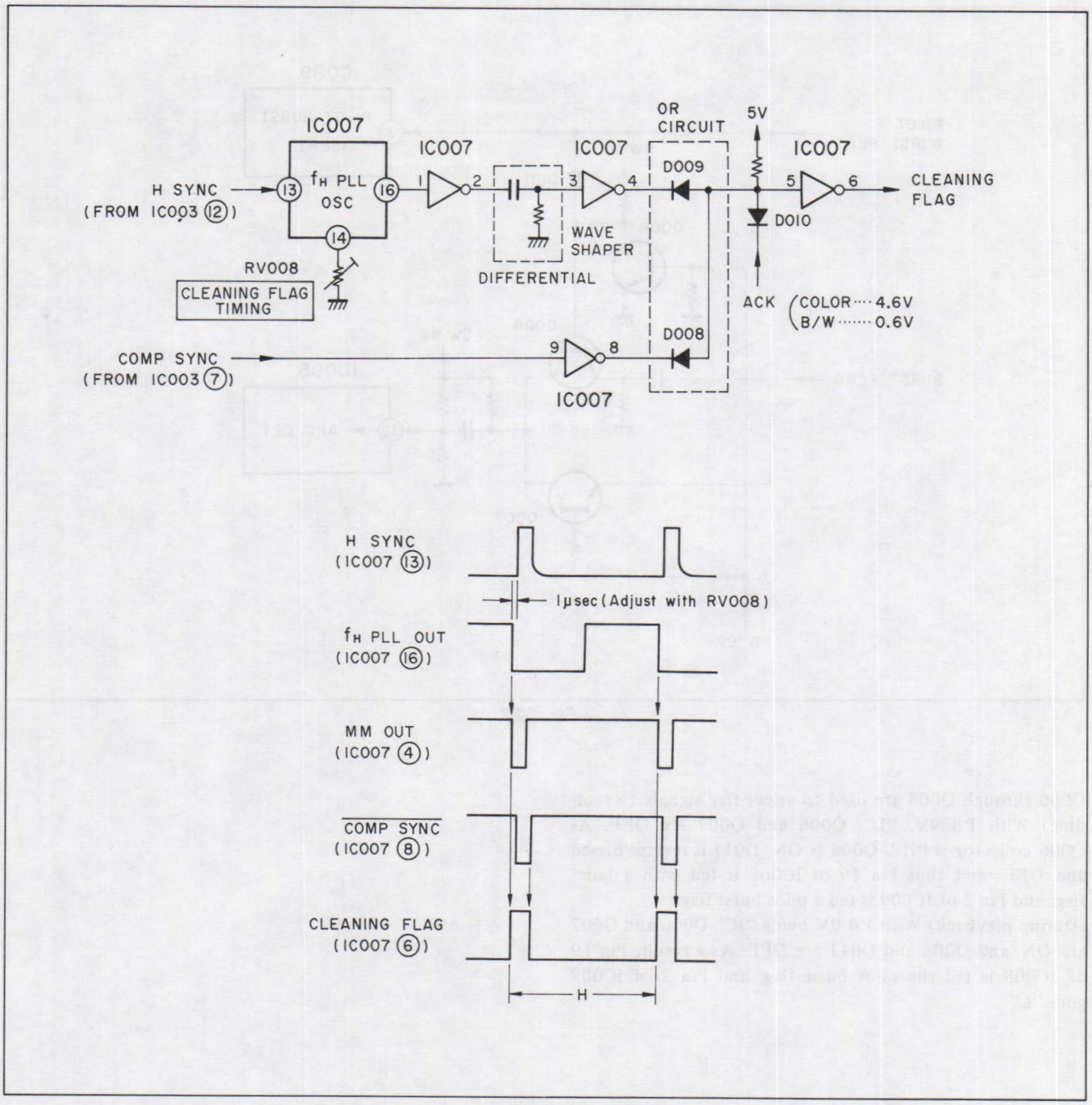


Fig. 1-26.

This flag is a pulse which is "H" during the horizontal sync period. It is wider than the horizontal sync signal to ensure cleaning of the pilot burst signal. The oscillation of the PLL oscillator in IC007 is synchronous with the horizontal sync signal. RV008 is used to control the leading edge of the output from Pin 16 to be 1 μs earlier than the leading edge of the horizontal sync signal. The output from Pin 16, fed through a monomultipulse, and the composite sync signal are combined to form the cleaning flag.

1-3-8. Flag Signal Selection Circuit

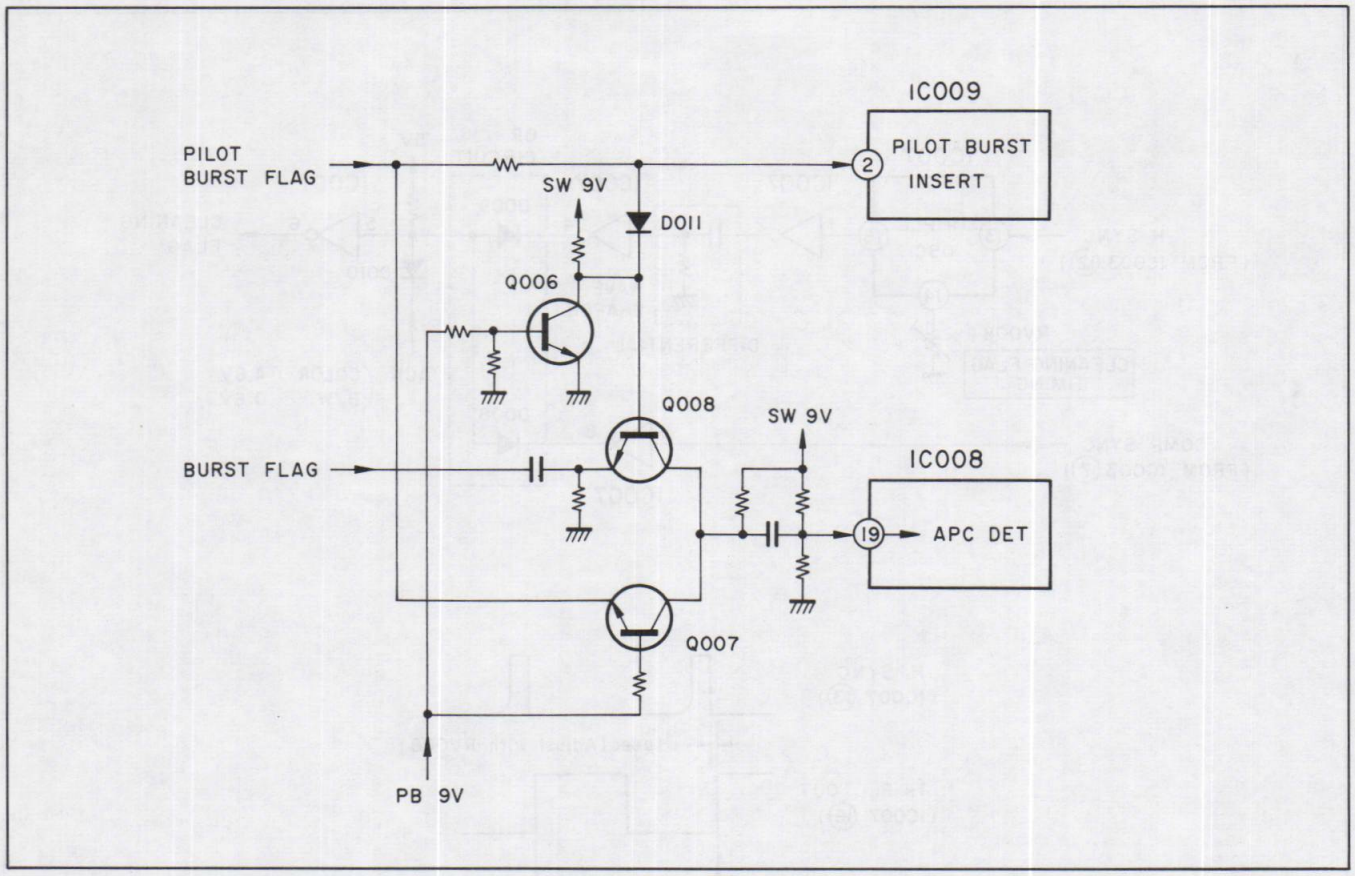


Fig. 1-27.

Q006 through Q008 are used to select flag signals. (Recording) With PB 9V, "L", Q006 and Q007 are OFF. As Q006 collector is "H", Q008 is ON, D011 is reverse biased and OFF; and thus Pin 19 of IC008 is fed with a burst flag, and Pin 2 of IC009 is fed a pilot burst flag.
(During playback) With PB 9V being "H", Q006 and Q007 are ON, and Q008 and D011 are OFF. As a result, Pin 19 of IC008 is fed the pilot burst flag, and Pin 2 of IC009 goes "L".

1-4. VARIABLE SPEED CHROMA PROCESS CIRCUIT

In the PAL system, the hue distortion is reduced by the use of the R-Y signal out of two color difference signals, or the R-Y and B-Y signals. Every one H (one line), the R-Y signal is inverted in phase, then suppressed carrier quadruple two-phases amplitude modulated. At the same time, the burst signal is changed in phase +135° and −135° from the reference phase Fig. 1-28.

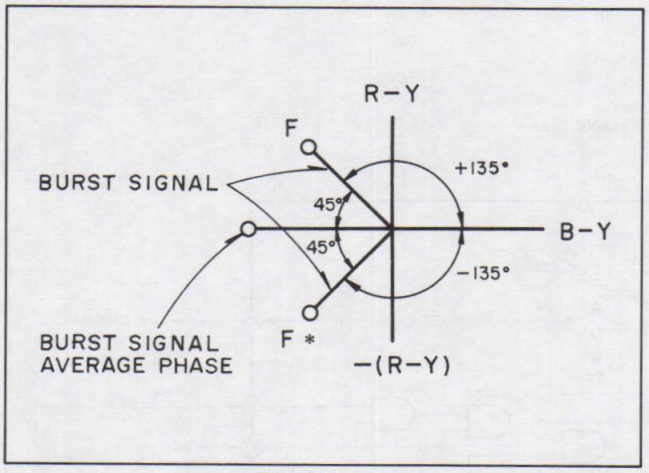


Fig. 1-28.

Assuming the line modulated with the (R-Y) signal to be F, and the line modulated with the -(R-Y) signal to be F*, the β-PAL tape format is expressed by Fig. 1-29.

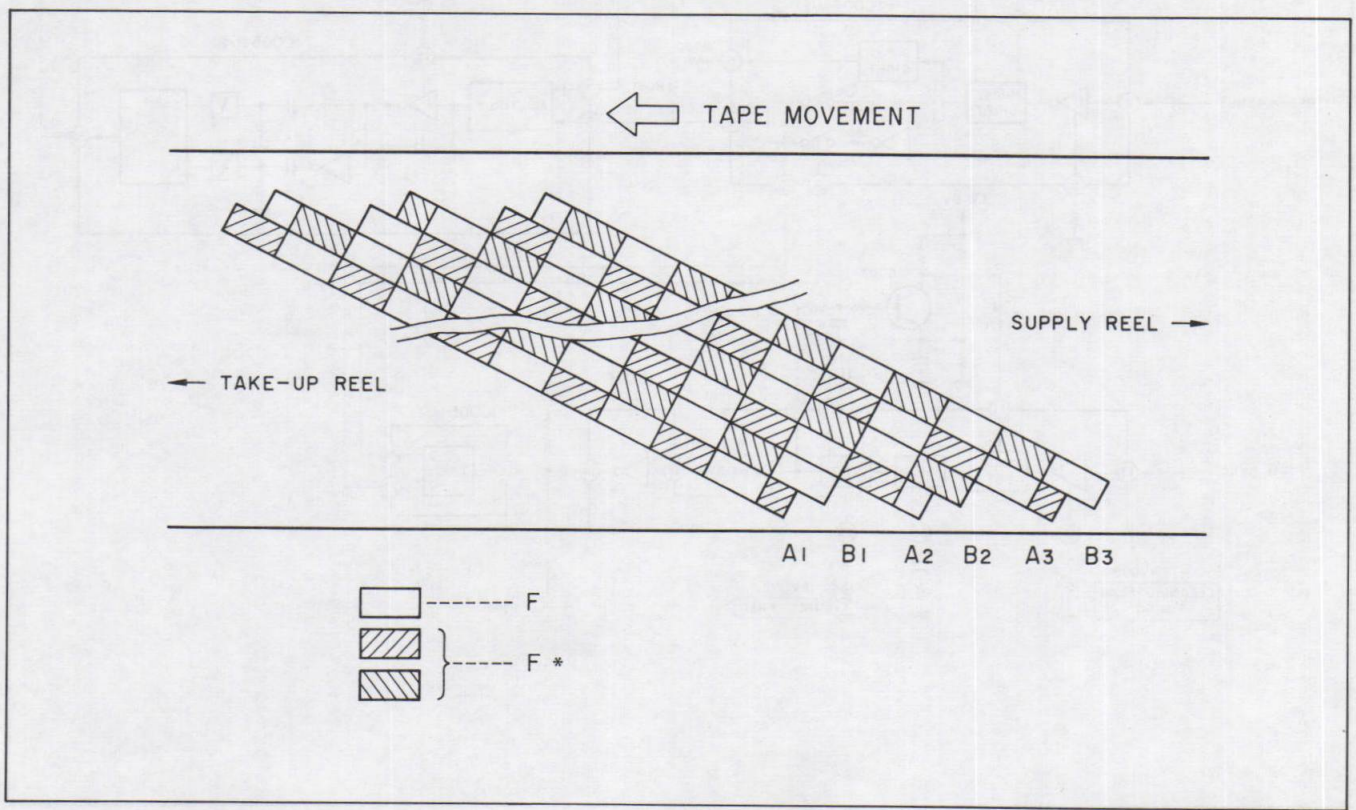


Fig. 1-29.

In variable speed playback such as for picture search, the video head on the tape will vary its track slope, and therefore, during one field, the video head will trace multiple tracks. As seen from the tape format, the Y-signal, with its orderly H alignment, will have no problem, but the chroma signal has no orderly arrangement in F and F* stated above. For example, when A1 and A2 tracks are compared, F and F* correspond in the adjacent tracks. (When the video head of channel A traces track B, the chroma signal of track B is canceled by the chroma-signal crosstalk cancel circuit; and so track B is ignored.) Therefore, when the video head tracing track A1 moves over track A2, lines F and F* exchange their alternate sequence. The R-Y signal will be inverted in phase from the normal signal. During variable speed playback, phase inversion will occur many times, and each time, the color will disappear and the complement color will appear. This must be corrected by a variable speed playback chroma process circuit.

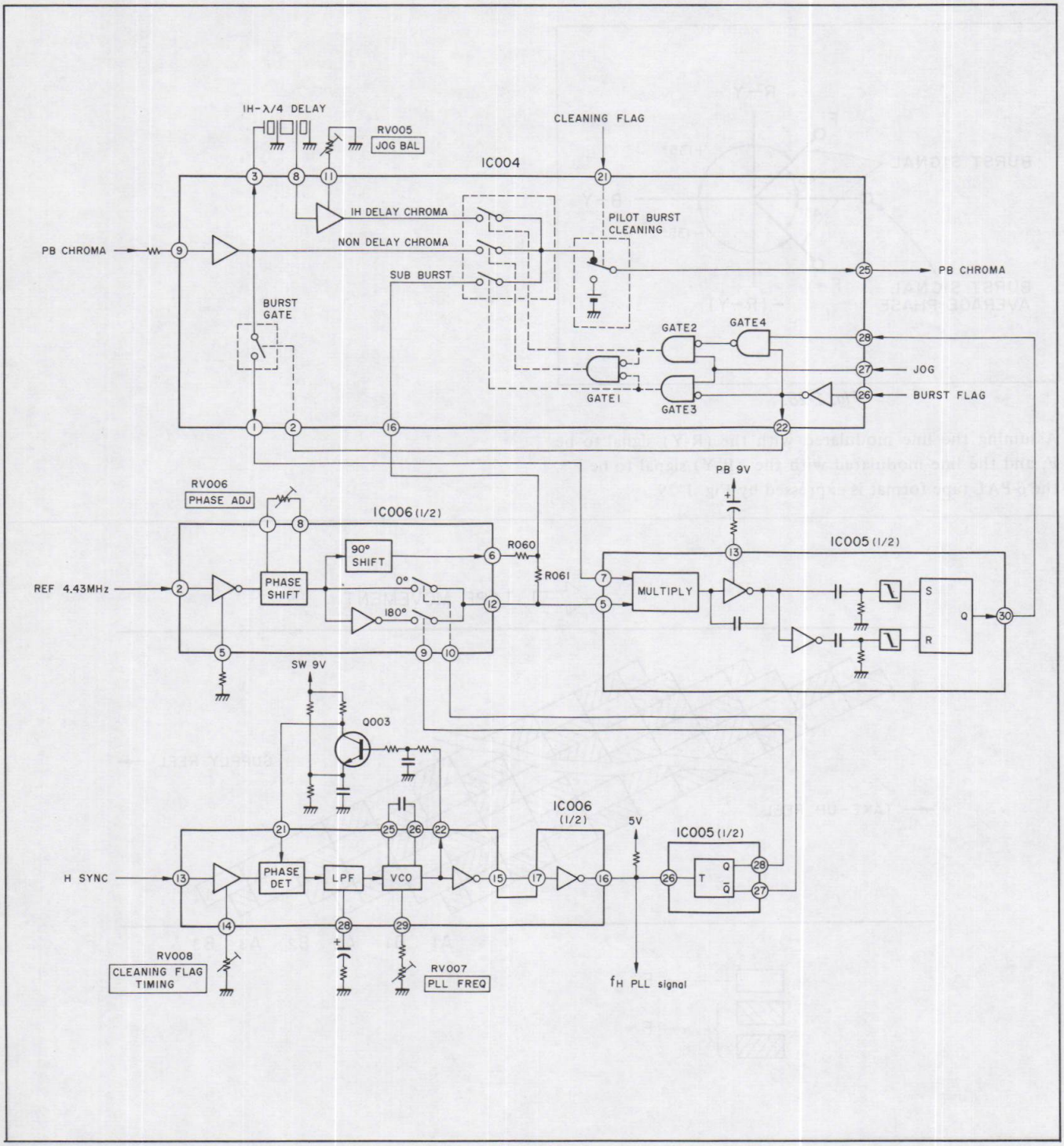


Fig. 1-30.

In this circuit, a sub-burst signal is generated from the output from the 1/2fH oscillator synchronized with the playback horizontal sync signal and from the 4.43 MHz signal, or the reference playback chroma frequency. This sub-burst signal has the same phase as that of the normal burst signal and is stable during variable speed playback. During variable speed playback, the sub-burst signal replaces the burst signal in the playback chroma signal. At the same time, the sub-burst signal and the playback signal are compared in phase; if the same phase, the playback chroma signal is output as is; if opposite phase, the chroma signal one H earlier that has passed the 1H delay circuit is output. In this manner, a chroma signal of normal phase is provided.

1-4-1. Phase Inversion Compensation Circuit

The playback chroma signal is input to Pin 9 of IC004. Here the signal is divided into three. From the first, only a burst signal is picked up by the burst gate, and is output from Pin 1 to the chroma phase discriminator. The second is output from Pin 3, delayed 1H, output from Pin 8 to enter the IC again, amplified, then level adjusted, and fed to the switch circuit in IC. The third is fed to the switch circuit directly. The switch circuit also receives the sub-burst signal from Pin 16. This switch circuit is controlled by the JOG signal, burst flag signal, and the output from the chroma phase discriminator (Pin 30 of IC005).

During normal playback, the JOG signal is "L", so the outputs from gates 2 and 3 are "L" and the output from gate 1 is "H", and therefore a non-delayed chroma signal is output.

During variable speed playback, the JOG signal is "H" and gates 2 and 3 are open. During the burst flag signal being "L" (period other than burst period), gate 4 is also open, and therefore, during the output from the Pin 30 of IC005 or discriminator being "H", gate 2 output is "H" and gate 1 output is "L", and as a result, a 1H delayed chroma signal is output from the switch circuit. During the output from Pin 30 being "L", gate 2 output is "L" and gate 1 output is "H", and thus a non-delayed chroma signal is output. During the burst flag signal being "H" (burst period), gate 4 is closed, gate 3 output is "H", gates 1 and 2 outputs are "L", and the sub-burst signal is output in place of the burst signal.

The output from the switch circuit is separated from the pilot burst signal by the cleaning flag input from Pin 21, and is output from Pin 25 of IC004.

1-4-2. Sub-burst Signal Generator Circuit

REF 4.43 MHz signal that is input to Pin 6 of IC006 is adjusted in phase in RV006 connected to Pins 1 and 8, and then divided in two. The first is inverted in phase every H by a square wave with 1/2fH frequency synchronized with the horizontal sync signal that is input to Pins 9 and 10, and then output from Pin 12. The second undergoes a 90° phase shift, and is output from Pin 6. RV006 controls the output from Pin 6 so that its phase is equal to the average phase of the playback burst signal. Then, the outputs from Pins 12 and 6 undergo a vector addition in R061 and R060 to provide the sub-burst signal.
In variable speed playback, this sub-burst signal, instead of the playback burst signal, is inserted into the chroma signal. The output from Pin 12 is used as the reference signal for the chroma phase discriminator.

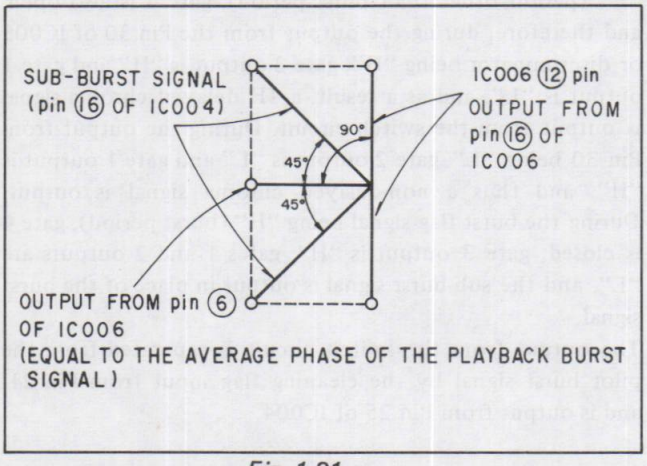


Fig. 1-31.

1-4-3. Chroma Phase Discriminator

During variable speed playback, a sub-burst signal, instead of the burst signal, is inserted into the chroma signal, and becomes the reference signal for the phase discrimination. To discriminate the phase of the playback chroma signal, Pin 7 of IC005 is receiving the playback burst signal from Pin 1 of IC004. The playback burst signal is shifted in phase +45° or −45° from the average phase of the sub-burst signal. Pin 5 of IC005 is receiving, as reference, the output from Pin 12 of IC006. This reference signal, synchronized with the sub-burst signal, is shifted phase +90° or −90° from the average phase of the sub-burst signal.
The playback burst signal and reference signal are compared in phases in a multiplier. The phase difference in these two signals is either 45° or 135°. When the phase difference is 45°, or the sub-burst signal and the playback burst signal are in the same phase, the output from the multiplier (Pin 12) becomes a negative pulse of period 1H. When this pulse is used to reset the flip-flop, the output from Pin 30 of IC005 goes "L". When the phase difference is 135°, or the sub-burst signal and the playback burst signal are in opposite phase, the output from the multiplier is a positive pulse with a 1H period, and the output from Pin 30 of IC005 goes "H".

1-4-4. fH Oscillation Circuit

Half of IC006 constitutes the PLL fH oscillator. With this oscillator, the VCO output is returned, via Pin 22 and Q3, to the phase detector of Pin 21, and its phase is compared with that of the H sync signal input from Pin 13. This output is returned via a low pass filter to VCO to provide a square wave with frequency fH synchronized with H sync. This VCO output (Pin 16 of IC006) is input to a flip-flop (Pin 26 of IC005) and counted down to 1/2. This Q output (Pin 28 of IC005) is input to Pin 9 of IC006 and turns the 180° shift circuit ON, and $\overline{Q}$ output (Pin 27 of IC005) is input to Pin 16 of IC006 to turn the 0° shift circuit ON.

SECTION 2
SYSTEM CONTROL

2-1. OUTLINE OF SYSTEM CONTROL

The system control operations are performed primarily by 3 microcomputers. They are IC601 (CPU1), IC602 (CPU2) and IC603 (CPU3) on the SS-1 printed circuit board. Inputs to the system control microcomputers include information generated by the function keys on the front panel, mechanical switches, abnormality detection signals from the servo block, the reel servo block, and input signals from the tuner/timer unit and camera. These three microcomputers process the input signals and generate the correct output signals for proper operations. The signals from the system control are sent to the servo, video, reel servo, and audio blocks. These signals are also sent to the LED and counter displays on the front panel, to solenoids, the loading and threading motor drive, video camera, changer connector output. Almost all operations of this unit are controlled by signals from these three microcomputers.

Figure 2-1 outlines the system control and input and output signals.

One characteristic of this unit is that the reels are driven by two reel motors, one for the supply reel and the other for the take-up reel. For this reason, system control performs almost no mechanical operations. Mechanical sections of the system control are the cassette loading mechanism, the tape threading mechanism, brake solenoid (to apply braking to the reels), and pinch solenoid (to clamp and release the pinch roller). These solenoids are of the self-latching type. Once a pulse voltage (200 msec) is given, the solenoids are magnetized or demagnetized, to maintain that status. Fig. 2-2 is a layout diagram of motor sensors. Sensors include a tape end sensor. No sensor has been provided for detection of tape slack as reel motor revolutions are detected only during FF and REW.

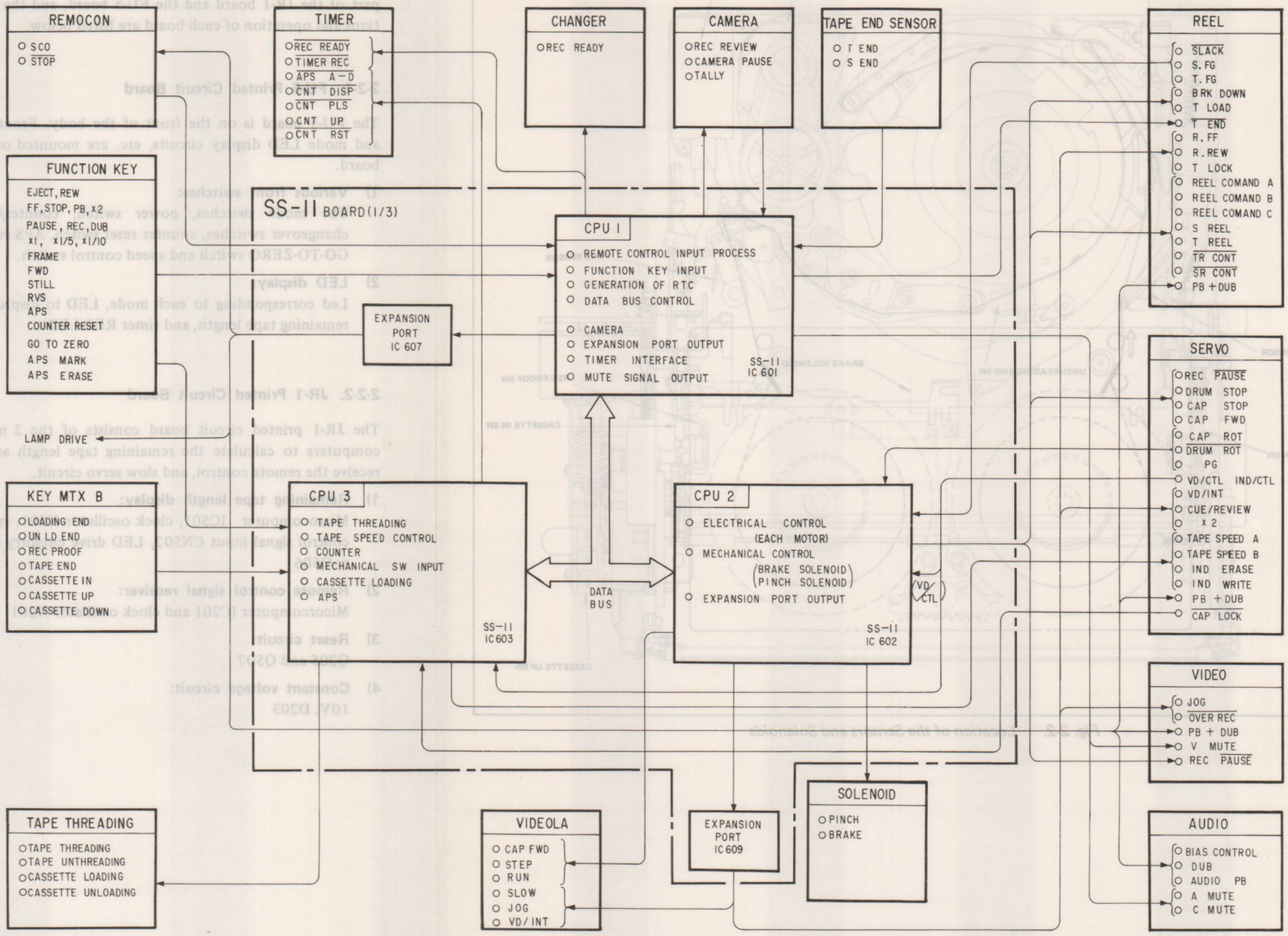


Fig. 2-1. CPU Input and Output Signals

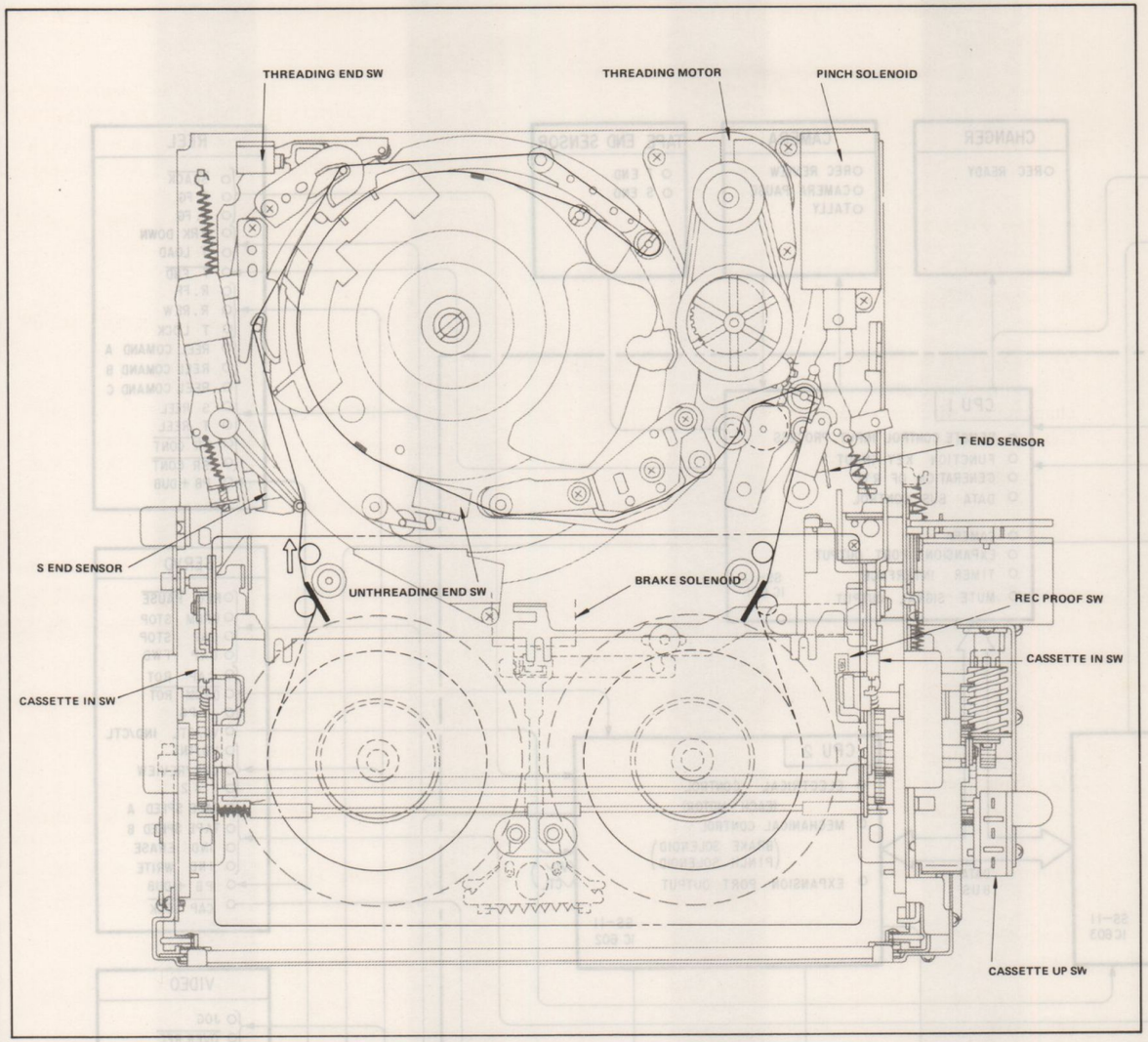


Fig. 2-2. Location of the Sensors and Solenoids

2-2. BLOCKS COMPRISING THE SYSTEM CONTROL

System control circuitry is found on the SS-11 board, and part of the JR-1 board and the FU-5 board, and the functions and operation of each board are listed below.

2-2-1. FU-5 Printed Circuit Board

The FU-5 board is on the front of the body. Front SWs and mode LED display circuits, etc. are mounted on this board.

1) **Various front switches:**
The mode switches, power switch, counter/timer changeover switches, counter reset switch, APS switch, GO-TO-ZERO switch and speed control switch.

2) **LED display:**
Led corresponding to each mode, LED to display the remaining tape length, and timer REC LED.

2-2-2. JR-1 Printed Circuit Board

The JR-1 printed circuit board consists of the 2 microcomputers to calculate the remaining tape length and to receive the remote control, and slow servo circuit.

1) **Remaining tape length display:**
Microcomputer IC501, clock oscillator X501, system control signal input CN502, LED drive circuitry Q501 ~ Q506

2) **Remote control signal receiver:**
Micorcomputer IC201 and clock oscillator X201

3) **Reset circuit:**
Q205 and Q507

4) **Constant voltage circuit:**
10V, D203

2-2-3. SS-11 Printed Circuit Board, System Control Unit

The system control on the SS-11 PC board consists of IC for control IC601 (MB88401-127), IC602 (MB88401-128), IC603 (MB88401-129), and IC's for output expansion such as IC607 and IC609, sensors and their level comparators, logic gate IC's IC606, 608, 611 and 612, etc.

1) **System control microcomputer:**
IC601, IC602 and IC603

2) **Expansion port:**
IC607 for IC601 output expansion and IC609 for IC602 output expansion

3) **End sensor circuit:**
IC605 to input data to IC601

4) **Reset circuit:**
IC604 (1/2)

5) **Index sense circuit:**
IC604 (1/2)

6) **Timing phase circuit:**
IC608 (1/2) to synchronize the REC.P signal with the CTL signal and IC608 (1/2) to synchronize the STEP signal with the PG signal.

7) **Changer (external controller) circuit:**
IC610

8) **Microcomputer oscillator:**
IC606 (2/6), X601 (4 MHz Xtal)

9) **Camera power supply and signal interface circuit:**
Q601 – Q606

10) **Cassette loading circuit:**
Q622 – Q627 IC611 (2/6), etc.

11) **Tape threading circuit:**
Q616 – Q621 IC611 (2/6), etc.

12) **Plunger drive circuit:**
Q612 – Q615 IC612 (4/6), etc.

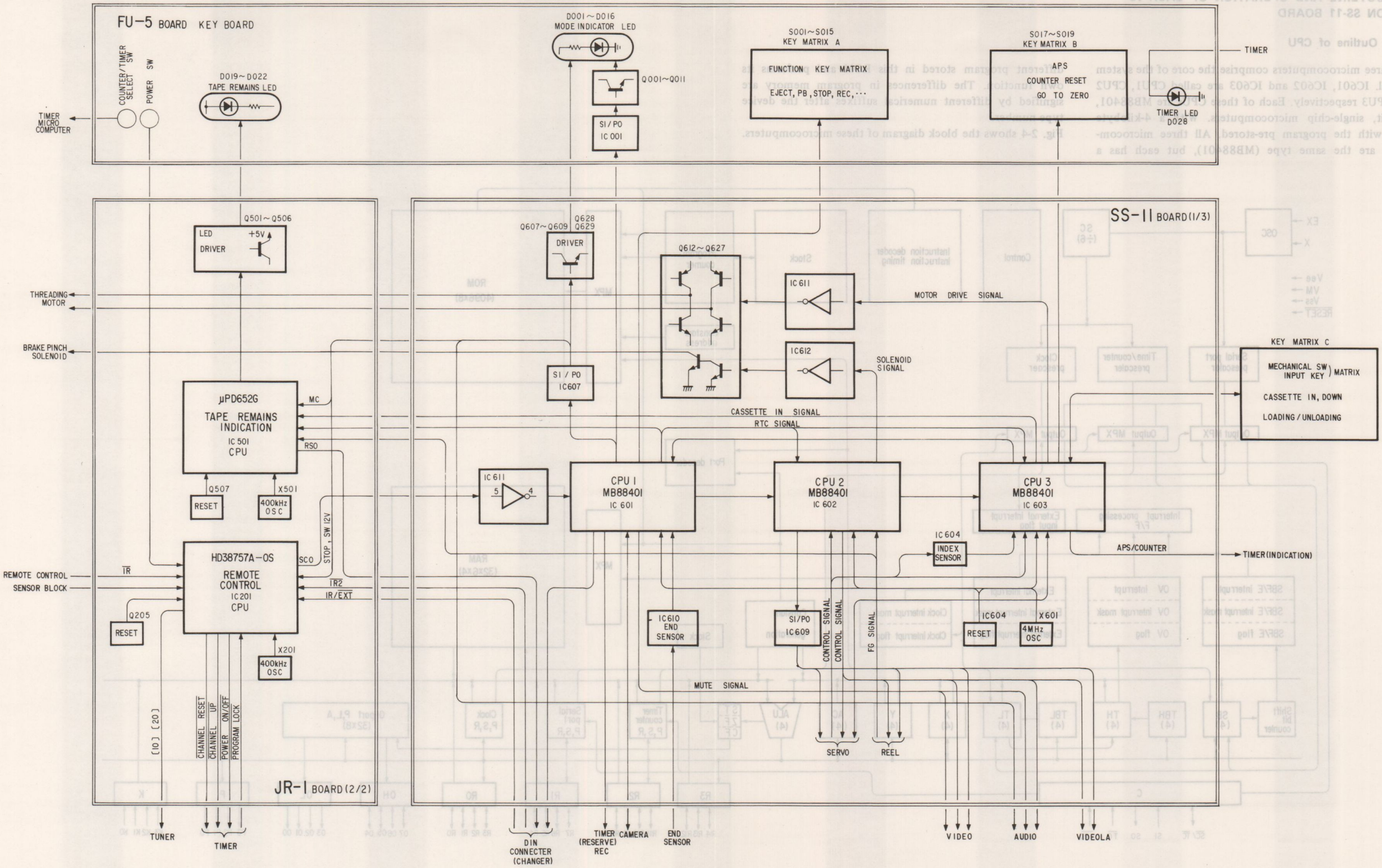


Fig. 2-3. System Control Block Diagram

2-3. OUTLINE AND OPERATION OF EACH IC ON SS-11 BOARD

2-3-1. Outline of CPU

The three microcomputers comprise the core of the system control. IC601, IC602 and IC603 are called CPU1, CPU2 and CPU3 respectively. Each of these CPUs are MB88401, four-bit, single-chip microcomputers. With a 4-kilobyte ROM with the program pre-stored. All three microcomputers are the same type (MB88401), but each has a different program stored in this ROM and performs its own function. The differences in program memory are signified by different numerical suffixes after the device type number.

Fig. 2-4 shows the block diagram of these microcomputers.

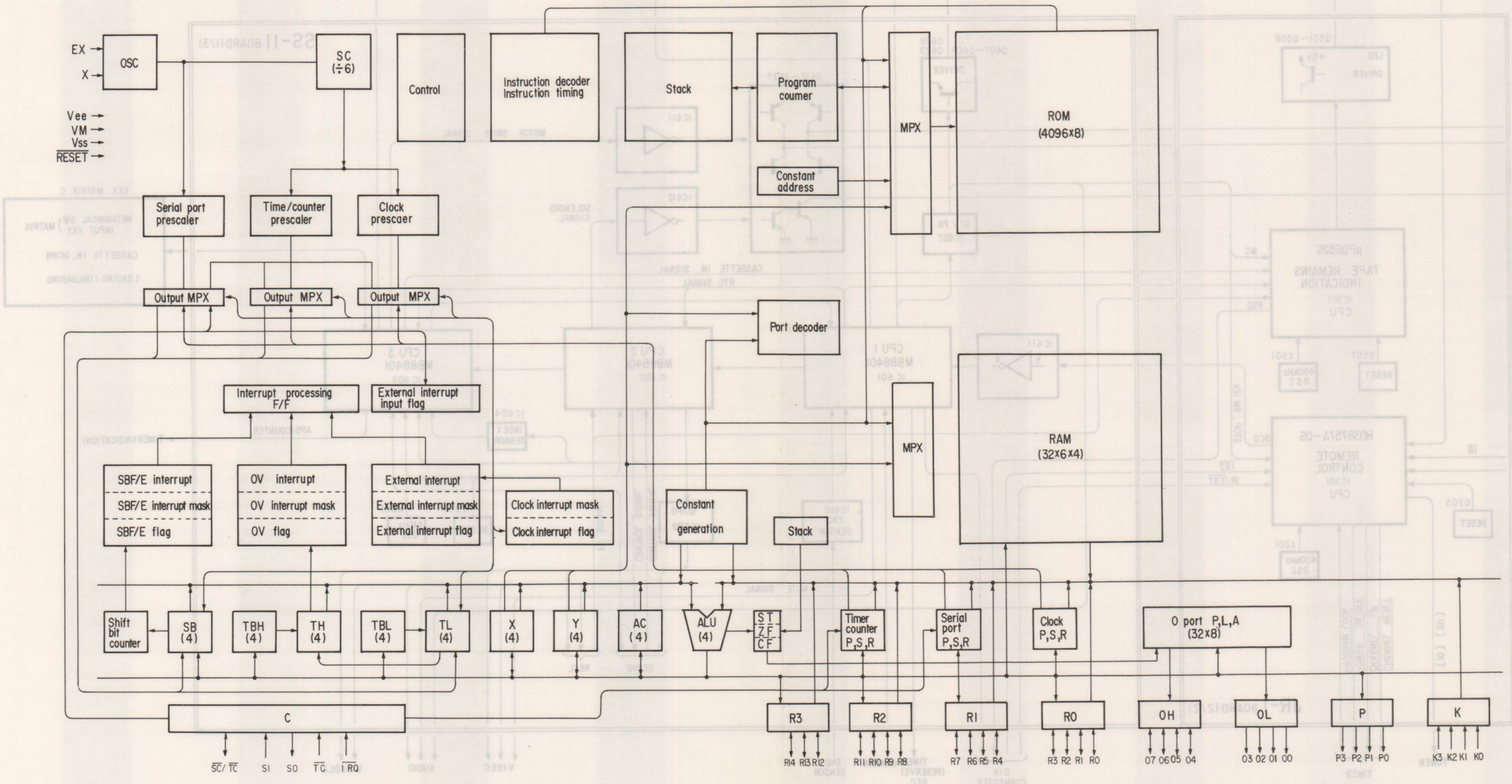


Fig. 2-4. MB8845 CPU Block Diagram

The features of this microprocessor are:

- ROM (read-only memory), 4096 words x 8 bits
- RAM (random-access memory, read/write memory), 192 words x 4 bits
- 6 storage registers, including accumulators
- 36 I/O (input/output) ports
- 1 serial input port
- 1 serial output port
- 1 interrupt port
- +5V operation
- High speed, minimum command execution of 3μs, 4 MHz clock
- N-MOS device
- 42-pin dual-inline design

The input and output ports are:

- K port (input port), 4 bits
- Ro – 14 ports (input and output ports), 15 bits
- OL, OH ports (output ports), 8 bits
- P port (output port), 4 bits
- C port (special port)

In this manual, names are given to these input and output ports according to their functions, and these ports are presented in tabular form for each CPU for ease of explanation.

"High" high-level signals are approximately 5V: "Low" low-level signals are approximately 0V. When a signal is low, its designation symbol has a bar over it, i.e. $\overline{\text{RQST}}$. I/O in these tables can be an input "I", or an output "O", relative to the CPU. The columns for destination are principal destinations. When there are several destinations, some destinations may be left out.

Fig. 2-5 shows the relationship between the three CPUs. Among these CPUs, CPU1 acts as a center to control CPUs2 and -3. A 400 Hz negative pulse RTC (real time control) signal is applied by CPU1 to the interrupt terminals (pin 19) of CPUs-2 and -3 to synchronize CPUs-2 and -3. Among the CPUs, data is transferred from CPU1→CPU2→CPU3→CPU1 making pins 24 and 23 the output and input respectively. Data are 4-bit serial data. When data are transferred, CPU1 generates a $\overline{\text{SC}}$ (shift clock) signal, which is a read pulse, to read data at the same time $\overline{\text{SC}}$ generated at pin 22 of CPU1 is sent to pins 22 of CPU2 and CPU3. System clock timing is set at 4 MHz by a crystal-controlled oscillator IC605 (1/5) and is sent to pin 20 EXTAL of CPU1, CPU2 and CPU3. Since all three CPUs are clocked together, data may be transferred synchronously, decisions may be made by each CPU, and outputs may be produced necessary for an operation relative to certain inputs.

When a function key on the front panel is pressed, for example, a signal is applied to CPU1 by the key matrix, and the data will be transferred from CPU1→CPU2→CPU3→CPU1. Each CPU will make a decision relative to the function selected. Inputs from mechanical switches are sent to CPU3; to transfer data, however, CPU3 requests CPU1 to issue data via a request command. This is the RQST (request) signal generated at CPU3 pin 1. After receiving this RQST signal, CPU1 transfers data in the order of CPU3→CPU1→CPU2→CPU3, and each CPU makes a decision to output signals as required.

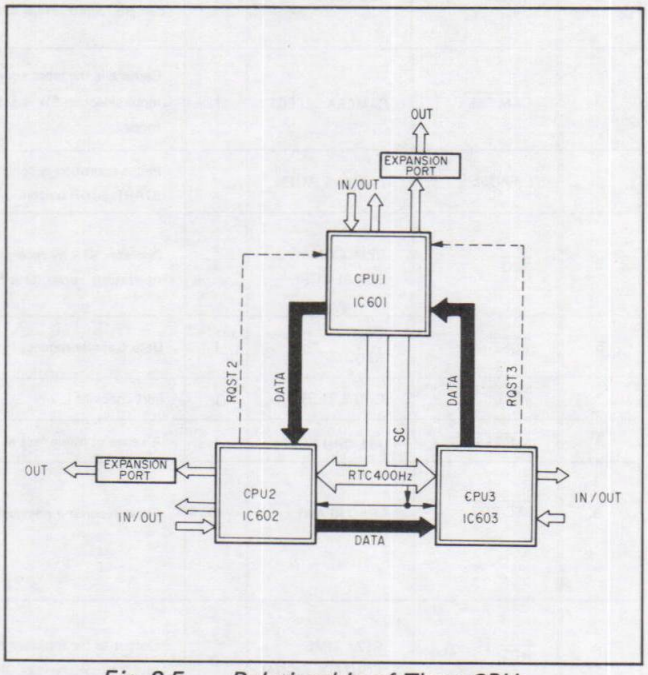


Fig. 2-5. Relationship of Three CPUs

2-3-2. Operation of CPU1 (SS-11 Printed Circuit Board, IC601)

1) Principal operations of CPU1

- CPU1 controls CPUs 2 and 3 and links the three CPUs together. This is achieved by sending an RTC signal to synchronize CPUs 2 and 3 with CPU1 so that data can be transferred between the S1 and S0 terminals (pins 24 and 23) of the CPUs. CPU1 also accepts an RQST (request) signal from the other two CPUs.
- CPU1 reads the mode commands from the function key matrix.
- CPU1 transmits data to the expansion port (IC607).
- CPU1 controls the timer block interface.
- CPU1 inputs data from and outputs data to the changers and controls such input/output.
- Camera control signals are received and transmitted.
- CPU1 reads and decodes the remote control input.
- Audio muting signals and video blanking signals are generated.
- The tape end output is monitored.

2) CPU1 pin functions

- SS-11 printed circuit board, IC601 MB88401-127

PIN No.	Designation	Meaning	I/O	Function and Operation	Signal	Connection
1	$\overline{\text{TM REC}}$	TIMER REC	I	Accepts instructions for timer-record only.	"L" in timer-record standby.	CN627 pin 2
2	R REV	REC REVIEW	I	REC review operation performed when camera record review button pushed.	"H" during REC review.	Camera RR SW from CN601 pin 4
3	$\overline{\text{CAM SEL}}$	CAMERA SELECT	I	Camera is the input source when the input selection SW is set in the camera mode.	"L" when the comera is used.	From CN613 pin 1 to INPUT SELECT SW
4	C PAUSE	CAMERA PAUSE	I	Pause operation is controlled by the camera START/STOP button.	"H" when the button is pressed.	Camera START/STOP SW from CN601 pin 2.
5	$\overline{\text{SCO}}$	REMOCON SERIAL CODE	I	Operates VTR by receiving renote control operation serial data from JR-1 board.	Serial bata.	From CN602 pin 1
6	$\overline{\text{RQST}}$	CPU REQUEST	I	Data transfer request from CPUs 2 and 3.	Negative pulse train.	CPU2 pin 40 CPU3 pin 1
7	$\overline{\text{TEST 1}}$	CPU 1 TEST	I	Port check at L.	Fixed at "H".	
8	$\overline{\text{ALL TEST}}$	ALL CPU TEST	I	A series of mode test at L.	Fixed at "H".	
9	$\overline{\text{REC RDY}}$	REC READY	O	Timer recording possibility indication	"L" for no cassette or cassette tab and tape end.	To IC610 pin 2
10	$\overline{\text{RTC}}$	REAL TIME CONTROL SIGNAL	O	Output to the interrupt terminals of OPU2 and 3 to synchronize CPU2 and 3.	400Hz negative pulse train.	CPU2 pin 19 CPU3 pin 19
11	AREC	AUDIO REC	O	Not used.	"H" during REC.	
12	$\overline{\text{KMIA 0}}$	KEY MATRIX INPUT A 0	I	Function key matrix input. (See appendix ; "Matrix Table")		Function key switch.
13	$\overline{\text{KMIA 1}}$	KEY MATRIX INPUT A 1	I	Function key matrix input. (See appendix ; "Matrix Table")		Function key switch.
14	$\overline{\text{KMIA 2}}$	KEY MATRIX INPUT A 2	I	Function key matrix input. (See appendix ; "Matrix Table")		Function key switch.
15	$\overline{\text{KMIA 3}}$	KEY MATRIX INPUT A 3	I	Function key matrix input. (See appendix ; "Matrix Table")		Function key switch.
16	Ex	Ex CLOCK	I	External clock input. (4 MHz)	4MHz	IC606 pin 10
17	X	X' tal CLOCK	O	Note connectable.		
18	$\overline{\text{RESET}}$	POWER ON RESET	I	IC604 inputs a 75 ms reset pulse to reset the CPU when the power is turned on.	About 75ms reset signal.	IC604 pin 1
19	$\overline{\text{T END}}$	TAPE END SENSOR	I	Information from the tape end sensor.	"L" at tape end.	IC 605 pin 2
20	$\overline{\text{TC}}$			NC		
21	Vss	GND		GND		GND
22	$\overline{\text{SC}}$	SHIFT CLOCK	O	Clock generation for data transfer.		CPU2 pin 22 CPU3 pin 22
23	DATA31	SERIAL DATA INPUT	I	Data transfer between CPUs, serial data from CPU3.	Serial data pulse train.	CPU3 pin 24
24	DATA12	SERIAL DATA OUTPUT	O	Data transfer between CPUs, receives serial data to CPU2.	Serial data pulse train.	CPU2 pin 23
25	$\overline{\text{KMOA 0}}$	KEY MATRIX OUTPUT A 0	O	Function Key switch output. (See appendix ; "Matrix Table")		Function key switch.

Table 2-1. (1/2)

26	$\overline{\text{KMOA 1}}$	KEY MATRIX OUTPUT A 1	O	Function Key switch output. (See appendix ; "Matrix Table")		Function key switch.
27	$\overline{\text{KMOA 2}}$	KEY MATRIX OUTPUT A 2	O	Function Key switch output. (See appendix ; "Matrix Table")		Function key switch.
28	$\overline{\text{KMOA 3}}$	KEY MATRIX OUTPUT A 3	O	Function Key switch output. (See appendix ; "Matrix Table")		Function key switch.
29	ExDATA 1	SERIAL PARALLEL PORT DATA	O	Sends data to the output expansion port.	Serial data pulse.	IC607 pin 16
30	Ex CLK 1	SERIAL PARALLEL PORT CLOCK	O	Synchronizes CLK send data to the output expansion port.	"H" during transmission.	IC607 pin 7
31	$\overline{\text{CSB}}$	SERIAL PARALLEL PORT CHIP SELECT B	O	Determines timing in conversion of parallel data of output expansion port FU-5 IC1.	"L" when selecting chip.	To CN002 pin 2 through IC606
32	$\overline{\text{CSC}}$	SERIAL PARALLEL PORT CHIP SELECT C	O	Controls the output expansion port (IC607) timing when converting to parallel data	"L" when selecting chip.	To IC607 pin 15 through IC605
33	V MUTE	VIDEO MUTING	O	Video muting signal output. 3 sec at start of PB mode.	"H" when V MUTE.	CN614 pin 4
34	C MUTE	CLICK MUTE	O	Mute with audio signal when changing operation mode.	"H" when C MUTE.	CN613 pin 6
35	A MUTE	AUDIO MUTING	O	Audio muting signal output. 3 sec at start of PB mode.	"H" when A MUTE.	CN613 pin 5
36	$\overline{\text{TALLY}}$	TALLY LAMP	O	Camera tally display output. Tally lamp is on during record.	"L" during REC, PB, DUB, ×2, CUE, REV.	From CN601 pin 3 to camera.
37	$\overline{\text{KMOA 4}}$	KEY MATRIX OUTPUT A 4	O	Function key switch output. (See appendix ; "Matrix Table")		Function key switch.
38	$\overline{\text{LOAD EN}}$	LOAD ENABLE	I	L : Key reception during EJECT. H : No Key reception during EJECT.	Fixed at "L"	
39	OPEN			Not connectable.		
40	SCO SMPL	SCO SAMPLING PULSE	O	Not used.		
41	VM			Internal RAM backup power supply.	+5V	
42	Vcc			Power supply.	+5V	

Table 2-1. (2/2)

- Function key matrix

	⑫ $\overline{\text{KMIA 0}}$	⑬ $\overline{\text{KMIA 1}}$	⑭ $\overline{\text{KMIA 2}}$	⑮ $\overline{\text{KMIA 3}}$
㉕ $\overline{\text{KMOA 0}}$	EJECT	STOP	FF	REW
㉖ $\overline{\text{KMOA 1}}$	PB	x 2	REC	PAUSE
㉗ $\overline{\text{KMOA 2}}$	DUB(R)	DUB(L+R)	—	—
㉘ $\overline{\text{KMOA 3}}$	RVS	STILL	FWD	—
㊲ $\overline{\text{KMOA 4}}$	FRAME	1/10	1/5	x 1

Table 2-2

2-3-3. SS-11 Board IC607 (MB8758)

This is a CMOS IC used as an output expansion port of CPU1. MB8758 is a serial/parallel conversion IC and operates as a decoder (serial/parallel conversion) when pin 14 is high, and as an encoder (parallel/serial conversion) when pin 14 is low. On this board, this IC is used only as a decoder by connecting +5V to pin 14. A clock is supplied by pin 30 of CPU1 to pin 7 and data are sent from pin 29 of CPU1 to pin 16.

The strobe signal of pin 15 is received from pin 32 of CPU1 ($\overline{CSC}$) for parallel output to pins 1 ~ 6 and 11 ~ 13. Figure 2-6 shows the relationship between serial and parallel data.

IC607 is used for control of LED indicators on the board and for control of the audio section.

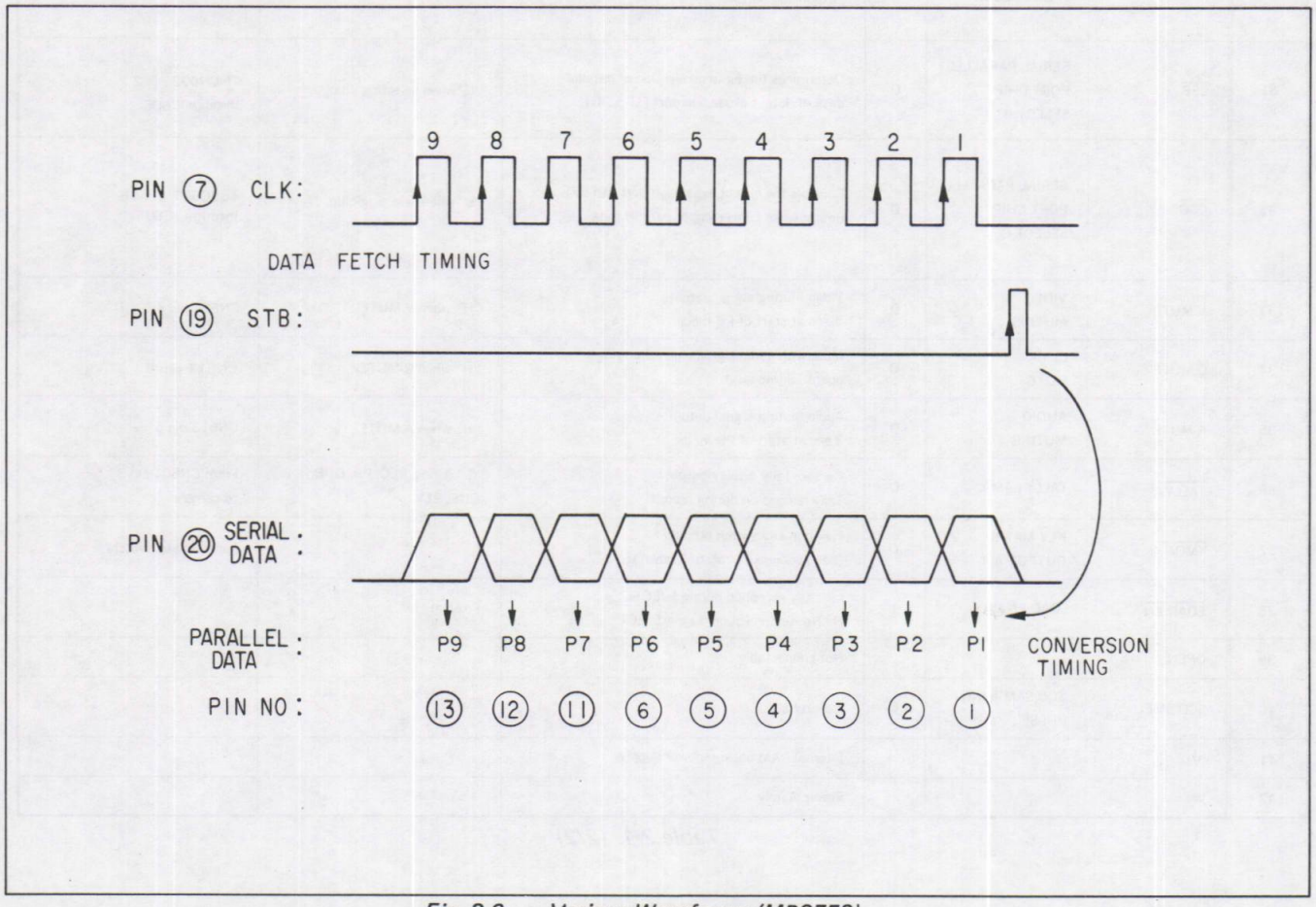


Fig. 2-6. Various Waveforms (MB8758)

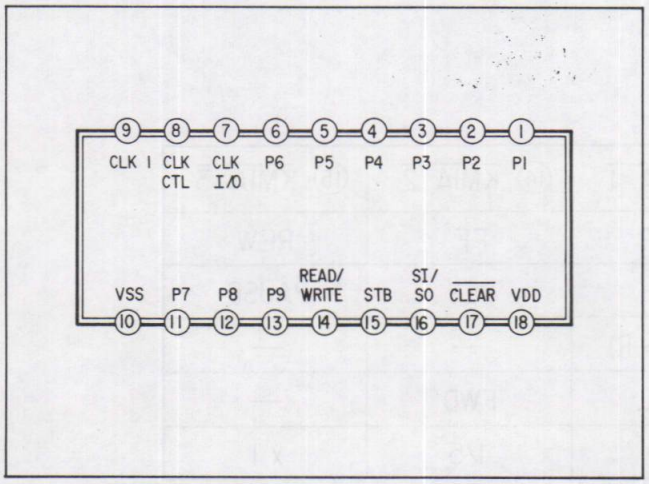


Fig. 2-7. Functions According to Pins

1) IC607 MB8758

PIN No.	Designation	Meaning	I/O	Function and Operation	Signal	Connection
1	REW	REW LED	O	REW LED drive.	"H" when lit.	LED via drive Tr.
2	FF	FF LED	O	FF LED drive.	"H" when lit.	LED via drive Tr.
3	PAUSE	PAUSE LED	O	PAUSE LED drive.	"H" when lit.	LED via drive Tr.
4	DUB R	DUB R LED	O	DUB R LED drive.	"H" when lit.	LED via drive Tr.
5	DUB L	DUB L LED	O	DUB L LED drive.	"H" when lit.	LED via drive Tr.
6	STOP	STOP	O		"L" when stopped.	to JR-1 PC board.
7	Ex CLK 1	CLOCK I/O	I	CPU 1 clock to drive MB8758.	Clock pulse.	CPU 1 pin 30 Ex CLK 1
8	CLK CTL	CLK CONTROL	I	H : CLK I/O is in input mode. L : CLK I/O is in output mode.	Fixed at "H".	+5V
9	CLK 1		I	Input port for clock Internal oscillation.	Fixed at "H". (Not used)	+5V
10	Vss			GND		GND
11	A PB	AUDIO PB	O	To switch audio REC/PB	"H" during PB.	CN613 pin 2
12	PB+DUB	PB+DUB	O	Mode signal during PB+DUB.	"H" when PB+DUB.	CN614 pin 3 CN623 pin 3
13	B CONT	BIAS CONTROL	O	Turns bias oscillator on during audio recording.	"H" during REC, DUB.	CN613 pin 4
14	R/W	READ,WRITE CONTROL	I	Switches between encoder and decoder operation. +5V is applied to use it as decorder.	Fixed at "H".	+5V
15	CSC	CHIP SELECT C (STB)	I	Controls the timing of data conversion into parallel by receiving strobe pulse from CPU 1.	"H" during strobe.	CPU 1 pin 32 $\overline{CSC}$
16	Ex DATA 1	Ex DATA 1	I	Serial data sent from CPU 1.	Serial data pulse train.	CPU 1 pin 29 From Ex DATA
17	$\overline{CLR}$	CLEAR	I	Reset pulse input.	Reset pulse	IC604 pin 1
18	Vdd			+5V power supply.		+5V

Table 2-3.

2-3-4. CPU2 (SS-11 Board IC602) Operation

1) The principal functions of the CPU2 are as follows:

- Inputs and outputs signals to and from the servo and reel blocks and controls these blocks.
- Effects mechanical control; controls the brake and pinch solenoids.
- Controls the output of the expansion port (IC609)

2) CPU-2 pin function

- IC602 MB88401-128

PIN No.	Designation	Meaning	I/O	Function and Operation	Signal	Connection
1	REC P	REC PAUSE	O	REC PAUSE signal.	"L" for REC.	Video block Servo block
2	C FWD	CAPSTAN FWD	O	Controls the capstan motor direction.	CAPSTAN MOTOR "H": FWD "L": REW	Servo block IC307 pins 13,5 and 8 IC309 pin 18
3	STEP	CAPSTAN STEP	O	1 pulse step (capstan) per frame - slow servo	I pulse per frame.	CN625 pin 4
4	TOP/END	TAPE TOP END	O	Alternately operate T and S sides of the end sensor.	TOP "H" END "L"	IC605 pin 5
5	UP LMT		I		Fixed at "H"	
6	PG	RF SW PULSE	I	Video head switching pulse.	Pulse waveform output when drum rotates.	IC301 pin 39
7	T FG	TAKE UP REEL FG	I	FG signal from the take-up reel to indicate to the CPU that the reel is rotating.	60 pulses for each rotation of reel.	IC001 pin 7 reel block
8	S FG	SUPPLY REEL FG	I	FG signal from the supply reel to indicate to the CPU that reel is rotation.	60 pulses for each rotation of reel.	IC001 pin I reel block
9	RVN	REVERSE NORMAL	O	Head change control signal.		CN625 pin 8
10	TR CONT	T REEL CONTROL	O	Tape tension control in tape threading.	600ms negative pule.	To reel block
11	SR CONT	S REEL CONTROL	O	Tape tension control in tape threading.	100ms negative pulse.	To reel block
12	SLACK	SLACK SENSOR	I	Detection of tape slack only generated when when the reel rotation slows down in FF or REW mode.	"L" when slack sensed.	Reel block Q002-C
13	CAP ROT	CAPSTAN ROTATION SENSE	I	Informs the CPU that the capstan is rotating.	"H" with capstan rotation.	Servo block IC301 pin 23
14	DRM ROT	DRUM ROTATION SENSE	I	Informs the CPU that the drum is rotating.	"L" with drum rotation.	Servo block IC301 pin 27
15	TEST-2	CPU 2 TEST	I	Port check at "L".	Fixed at "H"	
16	Ex TAL	Ex CLOCK	I	External clock input	4MHz	Shared by CPUs 1 and 3
17	X	X' tal CLOCK	O	Not connectable		
18	RESET	POWER ON RESET	I	(Same as CPU 1)	About 75ma reset signal	Shared by CPUs 1 and 3
19	RTC	REAL TIME CONTROL	I	Synchronous signal controlled by CPU 1.	400Hz pulses.	CPU 1 pin 10
20	VD/CTL	VD(REC)/CTL(PB)	I	Reading of VD or CTL to set continuous timig.	VD, CTL	IC307 pin 4
21	Vss	GND		GND		GND
22	SC	SHIFT CLOCK	I	Data read pulses from CPU 1.	Pulses	CPU 1 pin 22
23	DATA 12	DATA 1→2	I	Data transfer between CPUs to receive data transferred from CPU 1.	Serial data pulse train.	CPU 1 pin 24
24	DATA 23	DATA 2→3	O	Data transfer between CPUs to send data to CPU 3.	Serial data pulse train.	CPU 3 pin 23
25	T REEL	TAKE UP REEL DRIVE	O	Controls the take-up reel motor.	T-reel motor on when "L".	Reel block CP007 pin 3

Table 2-4. (1/2)

26	$\overline{\text{S REEL}}$	SUPPLY REEL DRIVE	O	Controls the supply reel motor.	S-reel motor on when "L".	Reel block CP008 pin 3
27	CAP STOP	CAPSTAN MOTOR STOP	O	Issues a command to stop the capstan motor when in the STOP, FF, REW, LOAD or UNLOAD modes.	"H" to stop the motor.	Servo block IC305 pin 4
28	DRM STOP	DRUM MOTOR STOP	O	Issues a command to stop the drum motor when in the STOP, LOAD or UNLOAD modes.	"H" to stop the motor.	Servo block IC303 pin 1
29	$\overline{\text{BRK ON}}$	BRAKE ON	O	Energizes the brake solenoid off.	"L" for 200ms when on-off	BRK plunger drive.
30	$\overline{\text{BRK OFF}}$	BRAKE OFF	O	Energizes the brake solenoid on.	"L" for 200ms when off-on	BRK plunger drive.
31	$\overline{\text{PINCH ON}}$	PINCH ON	O	Energizes the pinch solenoid on.	"L" for 200ms when off-on	PINCH plunger drive
32	$\overline{\text{PINCH OFF}}$	PINCH OFF	O	Energizes the pinch solenoid off.	"L" for 200ms when on-off	PINCH plunger drive
33	R COM A	REEL COMMAND A	O	Reel command output A. (See attached table)		Reel block IC006 pin 3
34	R COM B	REEL COMMAND B	O	Reel command output B (See attached code table)		Reel block IC006 pin 2
35	R COM C	REEL COMMAND C	O	Reel command out put C. (See attached code table)		Reel block IC006 pin 1
36	BRK DWN	BRAKE DOWN	O	Halves the braking power applied to the reel base to weaken the brake.		Reel block Q003-B
37	Ex DATA 2	SERIAL PARALLEL PORT A DATA	O	Output for serial data to the output expansion port IC.	Serial data pulse train.	IC609 pin 16
38	Ex CLK 2	SERIAL PARALLEL PORT A CLOCK	O	Supplies clock to the output expansion port IC.	Pulse	IC609 pin 7
39	$\overline{\text{CSA}}$	SERIAL PARALLEL CHIP SELECT A	O	Controls the output expansion port (IC603) timing when converting signal to parallel data.	Pulse	IC609 pin 15
40	RQST 2	CPU 2 REQUEST	O	Requests data transfer to CPU 1.	"H" when requested.	CPU 1 pin 6
41	V_M			Internal RAM back up power supply.		+5V
42	V_{CC}			+5V power supply.		+5V

Table 2-4. (2/2)

- Reel control instruction code table

	FWD	RVS	FF	REW	CUE	REV	THREADING UNTHREADING	STOP
(28) R COM A	L	H	L	H	L	H	L	H
(29) R COM B	L	L	H	H	L	L	H	H
(31) R COM C	L	L	L	L	H	H	H	H
BINARY →DECIMAL	0	1	2	3	4	5	6	7

Table 2-5.

2-3-5. IC609 MB8758

IC609 functions the same as IC607 on the output expansion port of the CPU1 and is used as an output expansion port for CPU2 primarily to control output signals to the reel and servo blocks.

1) SS-11 board IC609 MB8758

PIN No.	Designation	Meaning	I/O	Function and Qperation	Signal	Connection
1	SLOW	SLOW	O	Indicates a PB PAUSE state for still and slow playback.	"H" when still and slow PB mode.	Slow servo block CN625 pin 5
2	C/R	CUE + REVIEW	O	Indicates CUE and REVIEW operations.	"H" in CUE and REVIEW.	Servo block
3	JOG	JOG MODE	O	Occurs in variable speed PB mode.	"H" at variable speed PB mode.	Slow servo block CN625 pin 6
4	VD INT	VD INT	O	EXT, VD or INT VD switch output for REC and PB modes.	"H" in PB	Servo block
5	$\overline{\text{O REC}}$	OVER REC	O	Temporarily emphasizes recording when switched to record to produce a continuous recording.	"L" in recording with emphasis.	Video block CN614 pin 2
6	T LOCK	T REEL LOCK	O	Instructions to lock the T-reel generated in loading and unloading.	"H" when locked.	Reel block Q006-B
7	Ex CLK 2	Ex CLOCK 2	I	Clock drive input drive from CPU 2.	Clock pulse	CPU 2 pin 38
8	CLK CTL	CLOCK CONTROL	I	"H" : CLK I/O is input mode. "L" : CLK I/O is output mode.	Fixed at "H".	+5V
9	CLK 1		I	Input port for clock internal oscillation.	Fixed at "H" (Not used)	+5V
10	Vss	GND				GND
11	R FF	REEL FF	O	Reel motors are in FF.	"H" in FF mode.	Reel block Q007-B
12	R REW	REEL REW	O	Reel motors are in REW.	"H" in REW mode.	Reel block Q009-B
13	x2	x2 PB	O	Indicates double speed PB.	"H" when x2. (FWD and RVS)	Servo block Q332-B
14	R/W	READ/WRITE CONTROL	I	+5V always applied for serial to parallel decoder.	Fixed at "H"	+5V
15	CSA	CHIP SELECT A (STB)	I	Controls the timing of data transfer into the parellel register by receiving strobe from CPU 2.	"H" in strobe.	CPU 2 pin 39
16	Ex DATA 2	Ex DATA 2	I	Serial data input from CPU 2.	Serial data pulse train.	CPU 2 pin 37
17	$\overline{\text{CLR}}$	CLEAR	I	Reset pulse input.	"L" for 75ms when power is on.	IC604 pin 1
18	VDD			+5V power supply.		+5V

Table 2-6.

2-3-6. CPU3 (SS-11 Board IC603) Operation

1) The principal functions of the CPU3 are as follows:

- Controls cassette loading/unloading, tape threading/unthreading
- Controls tape speed
- Controls LCD counter display
- Inputs to mechanical switch matrix
- Auto program search

2) CPU3 pin function

- IC603 MB88401-129

PIN No.	Designation	Meaning	I/O	Funcion and Operation	Signal	Connection
1	RQST 3	CPU 3 REQUEST	O	Requests a command to transfer data from CPU 3 to CPU 1.	"H" when requested.	CPU 1 pin 6
2	OPEN			Not used.		
3	$\overline{\text{IND WRT}}$	INDEX WRITE	O	Index write signal.		To servo block
4	$\overline{\text{IND ERS}}$	INDEX ERASE	O	Index erase signal.	"H" during erase.	To servo block
5	INDCTL	INDEX CTL	I	For CTL duty signal.		IC307 pin 3
6	IND SNS	INDEX SENSE	I	Index sense input.	"H" during sense.	IC604 pin 7
7	CAP LCK	CAPSTAN LOCK	I	Capstan servo lock signal.	"H" during lock.	IC301 pin 21
8	$\overline{\text{CNT DISP}}$	COUNTER DISPLAY	I	Time display or counter display of the timer block display.	"H": Time display "L": Counter display	To timer block CN627 pin 6
9	OPEN			Not used.		
10	CNT UP	COUNTER UP	O	Decides whether the counter should count up or down.	"H": up "L": down	To timer blok CN627 pin 4
11	$\overline{\text{CNT PLS}}$	COUNTER PULSE	O	A pulse to change counter display.	"L" pulse	To timer block CN627 pin 3
12	$\overline{\text{KMIB 0}}$	KEY MATRIX INPUT B 0	I	Matrix input for the mechanical and counter switches. (see attached matrix table)		Mechanical switch, counter switch
13	$\overline{\text{KMIB 1}}$	KEY MATRIX INPUT B 1	I	Matrix input for the mechanical and counter switches. (see attached matrix table)		Mechanical switch, counter switch
14	$\overline{\text{KMIB 2}}$	KEY MATRIX INPUT B 2	I	Matrix input for the mechanical and counter switches. (see attached matrix table)		Mechanical switch, counter switch
15	$\overline{\text{KMIB 3}}$	KEY MATRIX INPUT B 3	I	Matrix input for the mechanical and counter switches. (see attached matrix table)		Mechanical switch, counter switch
16	Ex TAL	Ex CLOCK	I	External clock input.	4MHz	Shared dy CPUs 1 and 2
17	X	X'TAL CLOCK	O	Not connectable.		
18	$\overline{\text{RESET}}$	POWER ON RESET	I	(Same as CPU 1.)	About 75ms reset signal	Shared by CPUs 1 and 2
19	$\overline{\text{RTC}}$	REAL TIME CONTROL	I	A synchronous signal controlled by CPU 1.	400Hz pulse train.	CPU 1 pin 10
20	VD/CTL	VD/CTL	I	Reading VD/CTL to generate A MUTE and V MUTE signals.		
21	Vss			GND		GND
22	$\overline{\text{SC}}$	SHIFT CLOCK	I	Command to receive data from CPU 3.	Pulse train.	CPU 1 pin 22
23	DATA 23	DATA 2→3	I	Data transfer between CPUs. Data transfer from CPU 2.	Serial data pulse train.	CPU 2 pin 24
24	DATA 31	DATA 3→1	O	Data transfer between CPUs. Data transfer between CPU 1.	Serial data pulse train.	CPU 1 pin 23
25	TPSD A	TAPE SPEED A	O	Capstan speed control command A. (see attached matrix table.)		

Table 2-7. (1/2)

26	TPSD B	TAPE SPEED B	O	Capstan speed control command B. (see attached matrix trble.)		
27	CST IN	CASSETTE IN	O	Indicates cassette has been loaded.	"H" during cassette loading.	JR-1 board CN623 pin 7
28	$\overline{\text{CNT RST}}$	COUNTER RESET	O	Resets the counter.		To timer block CN627 pin 5
29	APS A	AUTO PROGRAM SEARCH A	O	Timer block APS displays binary signal. (see attached table)		CN620 pin 5
30	APS B	AUTO PROGRAM SEARCH B	O	Timer block APS displays binary signal. (see attached table)		CN620 pin 4
31	APS C	AUTO PROGRAM SEARCH C	O	Timer block APS displays binary signal. (see attached table)		CN620 qin 3
32	APS D	AUTO PROGRAM SEARCH D	O	Timer block APS displays binary signal. (see attached table)		CN620 pin 2
33	$\overline{\text{KMOB 0}}$	KEY MATRIX OUTPUT B 0	O	Matrix output of the mechanical and counter switches. (see attached matrix table)		Mechanical switch, counter switch
34	$\overline{\text{KMOB 1}}$	KEY MATRIX OUTPUT B 1	O	Matrix output of the mechanical and counter switches. (see attached matrix table)		Mechanical switch, counter switch
35	$\overline{\text{KMOB 2}}$	KEY MATRIX OUTPUT B 2	O	Matrix output of the mechanical and counter switches. (see attached matrix table)		Mechanical switch, counter switch
36	OPEN			Not used.		
37	$\overline{\text{T LOAD}}$	TAPE THREADING	O	Tape threading when a cassette is loaded.	"L" during threading.	From IC611 pin 2 to loading motor drive and reel block.
38	$\overline{\text{T UNLD}}$	TAPE UNTHREADING	O	Tape unthreading.	"L" during unthreading.	From IC611 pin 15 to loading motor drive.
39	$\overline{\text{C LOAD}}$	CASSETTE LOAD	O	Cassette loading motor drive signal.	"L" in cassette loading.	From IC611 pin 12 to loading motor drive.
40	$\overline{\text{C UNLD}}$	CASSETTE UNLOAD	O	Cassette loading motor drive signal.	"L" in cassette unloading.	From IC611 pin 10 to loading motor drive.
41	VM			Internal RAM backup power supply.		+5V
42	Vcc			+5V power supplv.		+5V

Table 2-7. (2/2)

- Capstan speed control instruction matrix

	X1	X2	CUE	REV	SLOW
㉕ TPSD A	L	H	L	L	L
㉖ TPSD B	H	L	L	L	H

Table 2-8.

- Mechanical switch matrix

	(12) $\overline{\text{KMIB 0}}$	(13) $\overline{\text{KMIB 1}}$	(14) $\overline{\text{KMIB 2}}$	(15) $\overline{\text{KMIB 3}}$
(33) $\overline{\text{KMOB 0}}$	CASSETTE IN	CASSETTE UP	CASSETTE DWN	REC PROOF
(34) $\overline{\text{KMOB 1}}$	MEMORY STOP	APS ERASE	APS	UNTHREADING END
(35) $\overline{\text{KMOB 2}}$	COUNTER CLEAR	APS MARK	TEST 3	THREADING END

Table 2-9.

- Index display table

INDEX 0	L	H	L	H	L	H	L	H	L	H	L	H	L	H
INDEX 1	L	L	H	H	L	L	H	H	L	L	H	H	H	H
INDEX 2	L	L	L	L	H	H	H	H	L	L	L	L	H	H
INDEX 3	L	L	L	L	L	L	L	L	H	H	H	H	H	H
DISPLAY	APS 0	APS 1	APS 2	APS 3	APS 4	APS 5	APS 6	APS 7	APS 8	APS 9	APS	APS ※1	※2	—

※1 Flashig
※2 During AUTO REWIND mode

Table 2-10.

2-4. SOLENOID DRIVE CIRCUITS

The unit has two solenoids of the self-latching type. The solenoids contain a latching magnet and operate by a current flow to the coils only when they change state (pulled in or released).

2-4-1. Pinch Solenoid Drive Circuit

Figure 2-8 is a pinch solenoid drive circuit. When the power is turned on, pin 31 of CPU2 ($\overline{\text{PINCH ON}}$) changes from high to low, and is inverted to high by inverter IC612. When Q613 turns on, a current from 12V is drawn through the pinch solenoid, and the solenoid is then latched by its magnet. (The signal output from CPU2 is on for approximately 200 ms.) When power is turned off, pin 32 of CPU2 ($\overline{\text{PINCH OFF}}$) turns low and Q612 turns on, turning off the pinch solenoid.

When the power supply is turned off, Q611 turns on while Q612 also turns on via R680. Therefore, the pinch solenoid is turned off positively by the hardware.

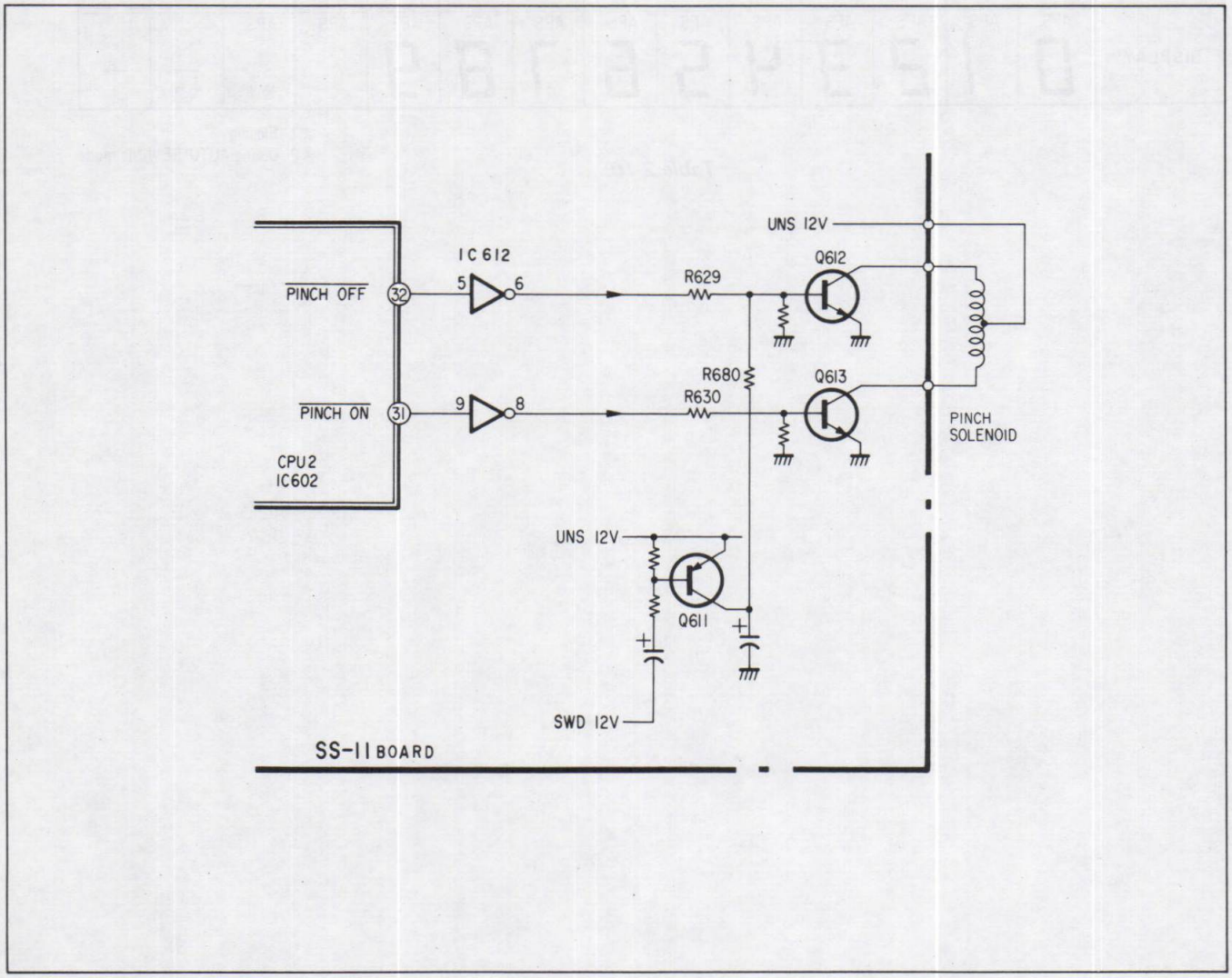


Fig. 2-8. Pinch Solenoid Drive Circuit

2-4-2. Brake Plunger Drive Circuit

Fig. 2-9 shows the brake solenoid drive circuit.

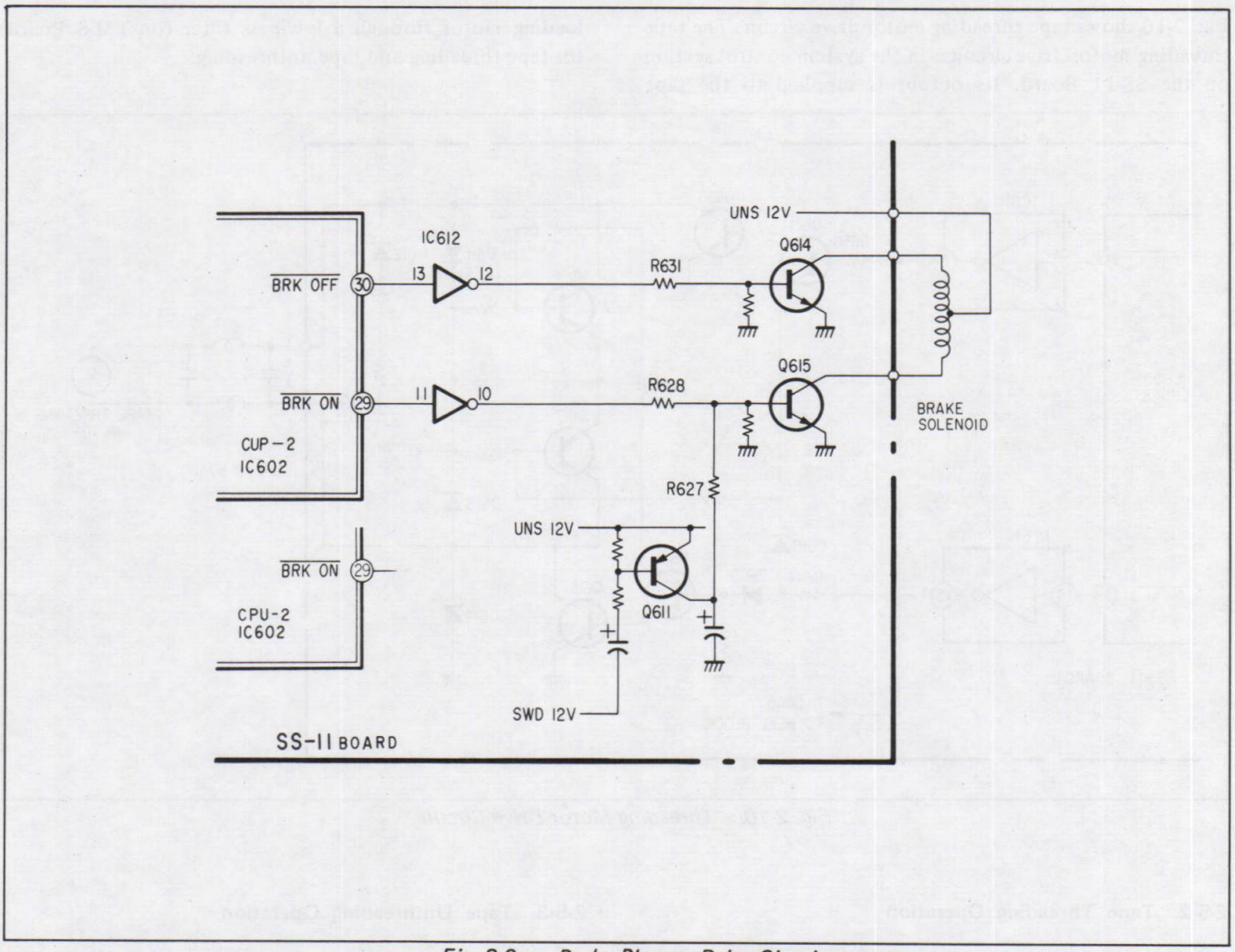


Fig. 2-9. Brake Plunger Drive Circuit

As is the case with the pinch solenoid, pin 30 of CPU2 goes "Low" for about 200 msc when it is in the OFF mode. Inverted by IC612, Q614 turns on, to turn off the brake solenoid.

In a normal ON operation, pin 29 of CPU2 turns "Low", and the signal passes through IC612, to turn on Q615, turning on the brake solenoid.

When the power supply is off, Q617 turns on, and the signal turns on Q615 through R627 causing the brake to operate.

2-5. THREADING MOTOR DRIVE CIRCUIT

2-5-1. Tape Threading Motor Drive Circuit

Fig. 2-10 shows tape threading motor drive circuit. The tape threading motor drive circuit is in the system control section on the SS-11 Board. Its output is supplied to the tape loading motor through a low-pass filter (on LM-8 Board) for tape threading and tape unthreading.

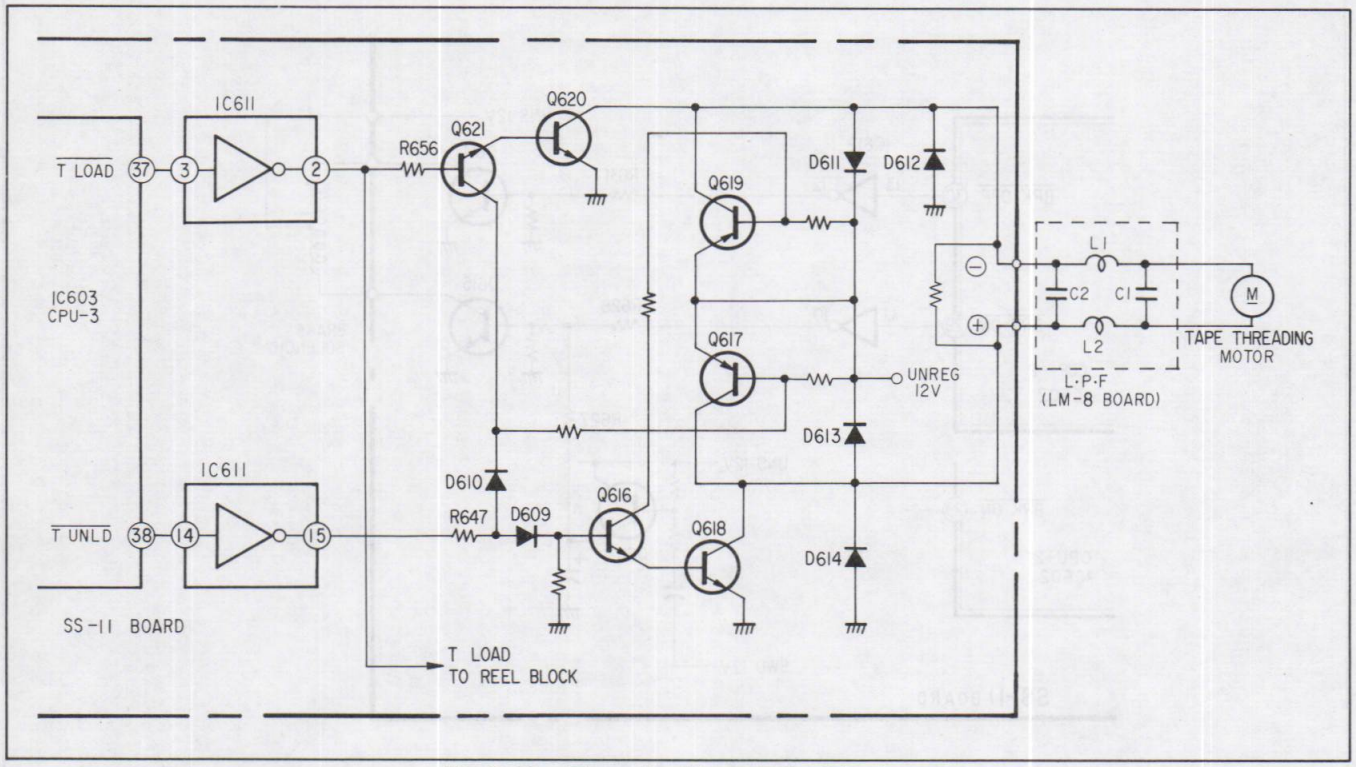


Fig. 2-10. Threading Motor Drive Circuit

2-5-2. Tape Threading Operation

When tape threading, pin 37 of CPU2 ($\overline{\text{T-LOAD}}$) turns low. The signal path is as follows: CPU2 pin 37 low. IC611 pin 2 high R656 Q621 on Q620 on. The collector of Q620 and the (–) side of the tape threading motor go low.
12V is applied to the emitter of Q617. When Q621 is turned on, Q617 turns on, to feed a high signal to the (+) side of the tape threading motor to perform the tape threading operation.

The states of Q616 to Q621 are shown in the table below. D611 to D614 are used for protection when the low pass filter is charging or discharging.

Q616	OFF	Q619	OFF
Q617	ON	Q620	ON
Q618	OFF	Q621	ON

D609 and D610 are Off

Table 2-11.

2-5-3. Tape Unthreading Operation

When tape unthreading, pin 38 ($\overline{\text{T UNLD}}$) of CPU2 turns Low, and the signal path is as follows: CPU2 pin 38 low→ IC611 pin 15 high→R647→D609→Q616 on→Q618 on. The collector of Q618 and the tape threading motor (+) side become low. 12V is applied to the emitter of Q619. Since Q616 is on, Q619 turns on, and its collector and the (–) side of the tape threading motor become high to initiate tape unthreading. The states of Q616 to Q621 are shown in the table below.

Q616	ON	Q619	ON
Q617	OFF	Q620	OFF
Q618	ON	Q621	OFF

D610 is on and D609 is Off

Table 2-12.

D609 and D610 are inserted to protect the transitors from damage. These diodes will conduct in an abnormal condition when both $\overline{\text{T UNLD}}$ and $\overline{\text{T LOAD}}$ become "Low" at the same time. In this case, $\overline{\text{T LOAD}}$ operates preferentially.

2-5-4. Cassette Loading Drive Circuit

Fig. 2-11 shows the cassette loading motor drive circuit. Its circuit configuration and operation are the same as those of the tape threading drive circuit, and their description will be omitted.

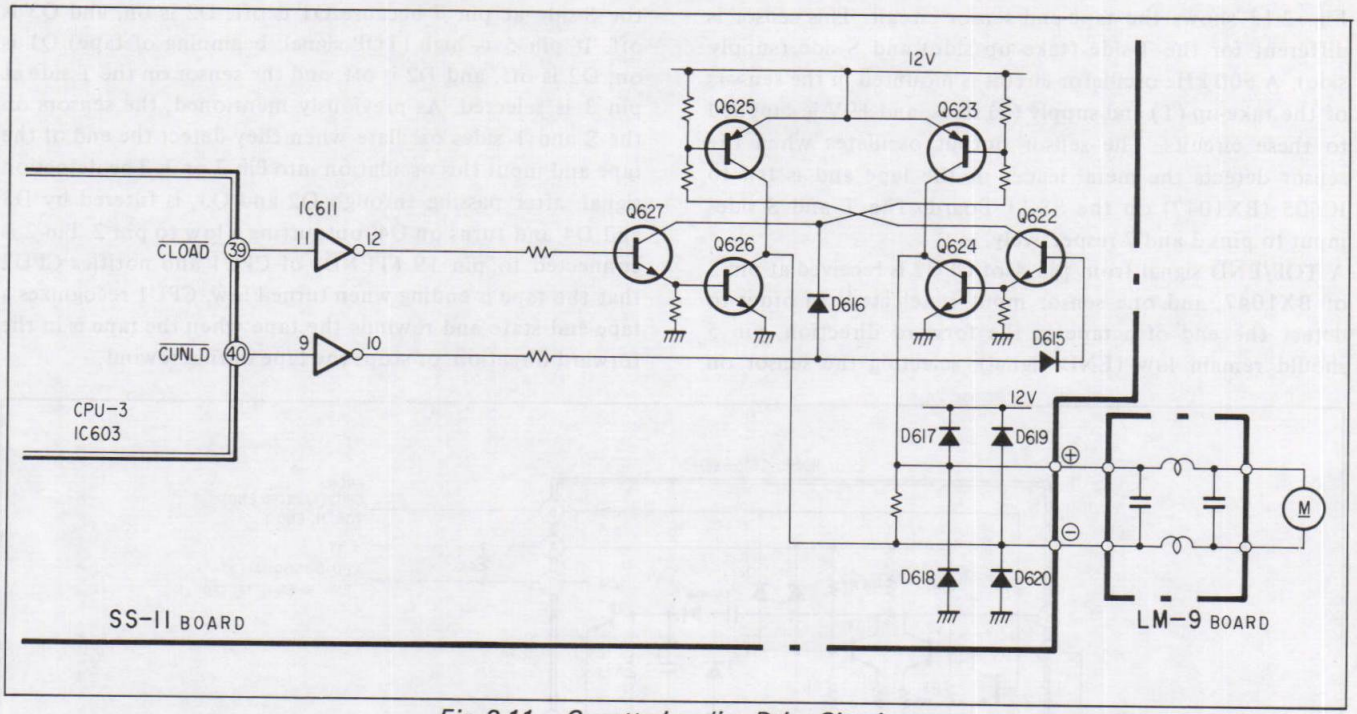
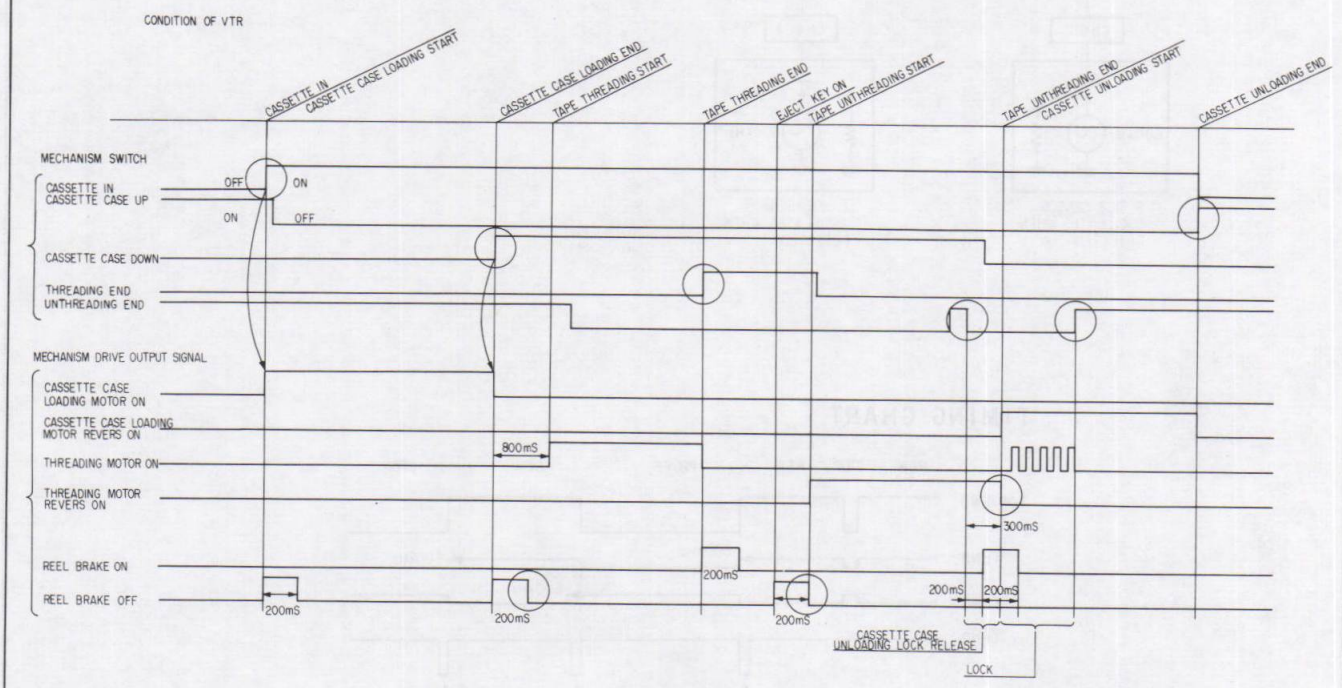


Fig. 2-11. Cassette Loading Drive Circuit



Note:

1. Cassette case unloading lock release
   When setting the unload and switch from ON position to OFF position, the tape loading motor reverses (unloading) for 300 msec continuously.
2. Cassette case unloading lock reset
   After releasing the cassette case unloading lock, the tape loading motor forward rotation signal is turned on and off. The cassette case unloading lock is reset by the pulse drive.

Fig. 2-12. Loading/Unloading Control

2-6. SENSOR CIRCUIT

2-6-1. Tape-end Sensor

Fig. 2-13 shows the tape-end sensor circuit. This sensor is different for the T-side (take up side) and S-side (supply side). A 600 kHz oscillator circuit is mounted in the sensors of the take-up (T) and supply (S) sides, and +9V is supplied to these circuits. The sensor output oscillates when the sensor detects the metal leader of the tape and is fed to IC605 (BX1047) on the SS-11 Board. The T and S sides input to pins 3 and 7 respectively.

A TOP/$\overline{\text{END}}$ signal from pin 4 of CPU2 is received at pin 5 of BX1047, and one sensor input is selected. In order to detect the end of a tape in the forward direction, pin 5 should remain low (END signal), selecting the sensor on the S-side at pin 7 because Q1 is off, D2 is on, and Q3 is off. If pin 5 is high (TOP signal, beginning of tape) Q1 is on, Q2 is off, and D2 is off, and the sensor on the T side at pin 3 is selected. As previously mentioned, the sensors on the S and T sides oscillate when they detect the end of the tape and input this oscillation into Pin 7 or 3. The detection signal, after passing through Q2 and Q3, is filtered by D3 and D4 and turns on Q4, outputting a low to pin 2. Pin 2 is connected to pin 19 ($\overline{\text{TEND}}$) of CPU1 and notifies CPU2 that the tape is ending when turned low. CPU1 recognizes a tape-end state and rewinds the tape when the tape is in the forward direction, or stops the tape during rewind.

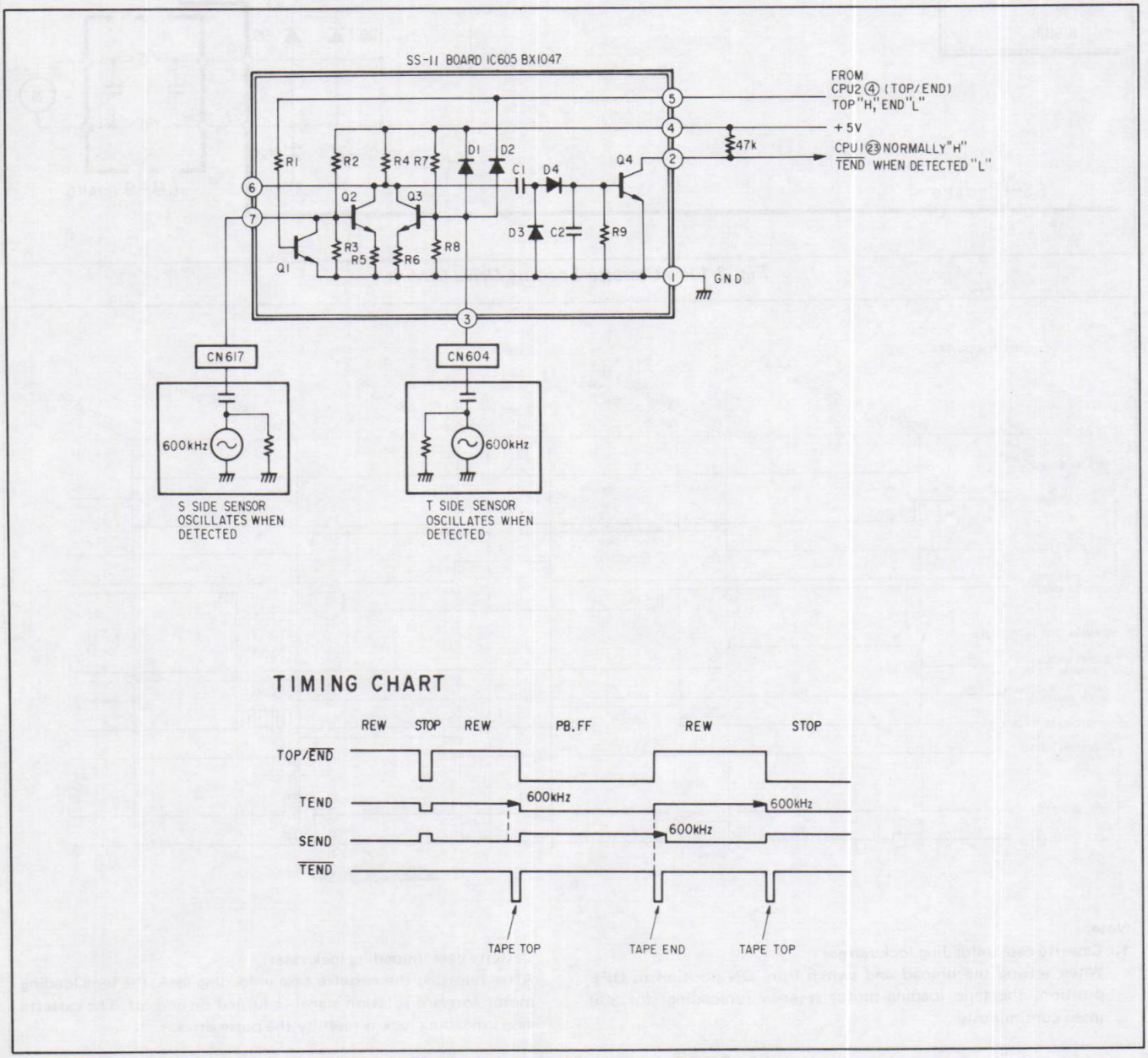


Fig. 2-13. Tape End Sensor Circuit

2-6-2. Index Sense Circuit

The index sense circuit detects the difference between normal CTL (50% duty) and CTL (20% duty) during index writing.

The index sense circuit integrates the CTL signal, converts it into a d.c. level, compares it, and inputs to pin 4 of IC603. By software programming, it does not monitor for one sec after mode conversion until the integration time constant stabilizes to the d.c. level.

Fig. 2-14 shows the circuit and timing chart.

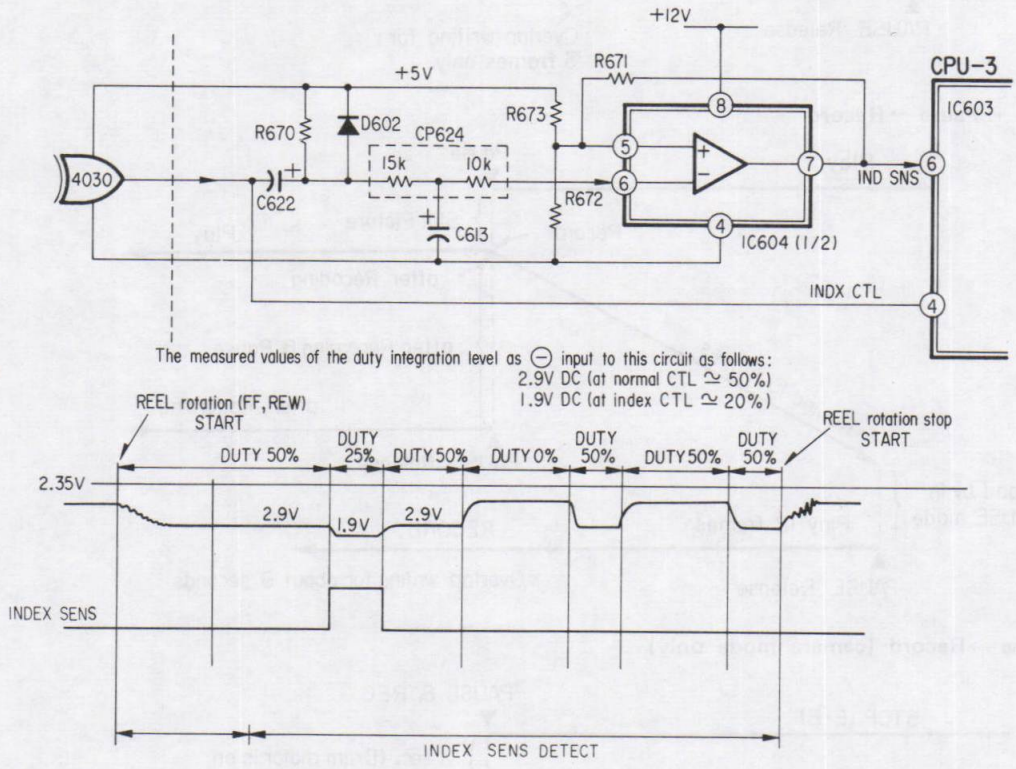


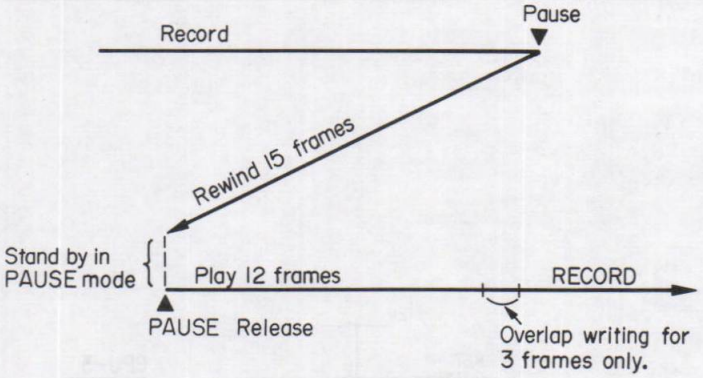
Fig. 2-14. Index Sense Circuit

2-7. OTHER CIRCUITS

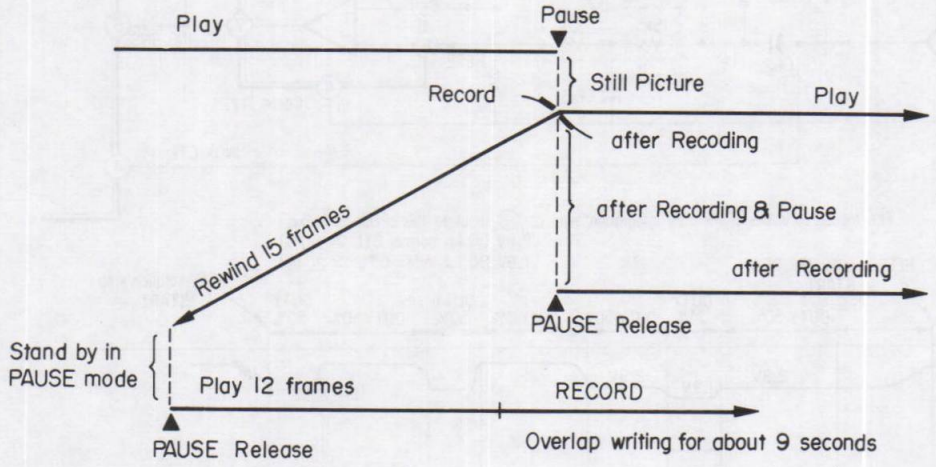
2-7-1. Editing Circuit

By pressing the pause button (REC + PAUSE), the tape is automatically rewound 15 frames before being set in the pause mode. When releasing pause to start recording, control (CTL) signals for the rewound portion are counted in order to maintain proper timing before the recording is started to ensure a smooth, distortion-free editing of the previously-recorded video.

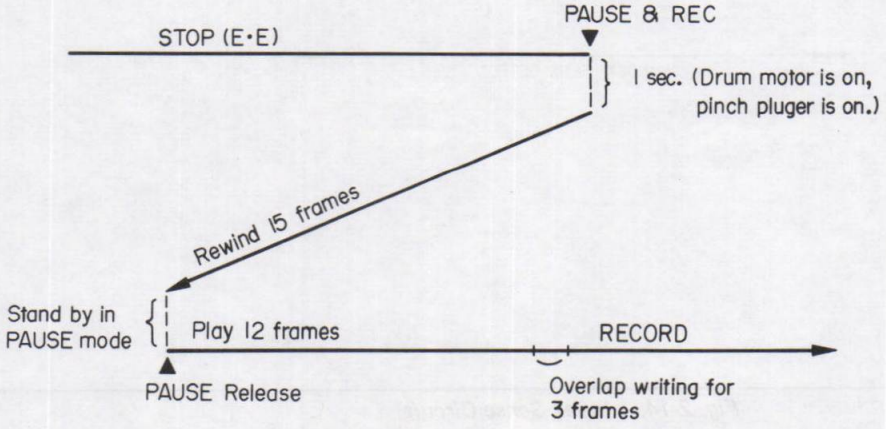
1) Record → Record + Pause → Record



2) Play → Play + Pause → Record

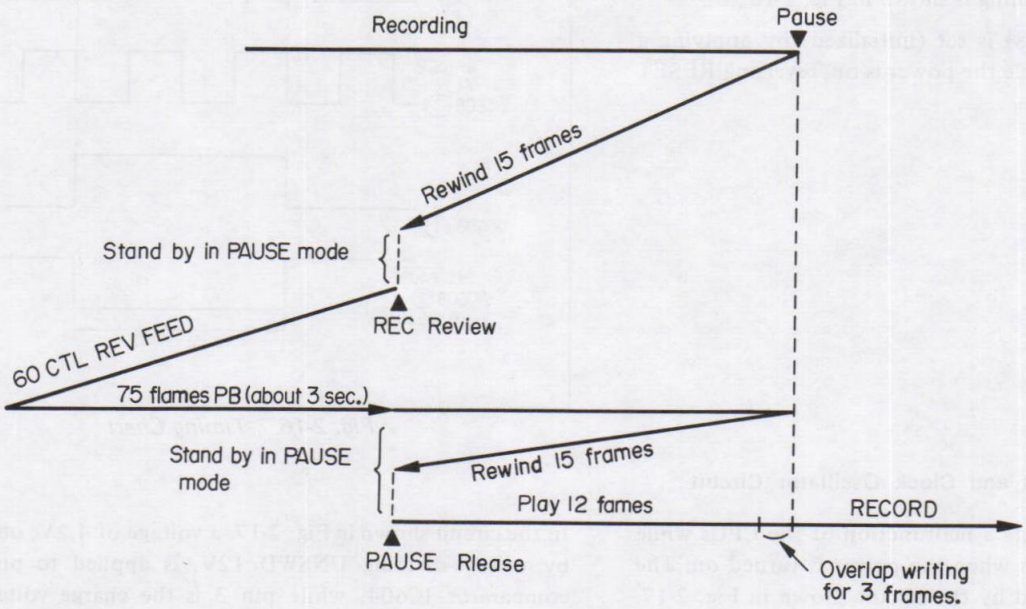


3) Stop → Pause → Record (camera mode only)



4) Record review function

By pressing the REC REVIEW button on the camera during REC + PAUSE mode, the last portion of the recorded scenes may be viewed for convenience in checking the recording.



- The preceding four editing operations are made by controlling the starting and stopping of the tape with the capstan motor while leaving the pinch solenoid on.
- Record review may be selected on during the REC + PAUSE mode and may be repeated.
- If the REC + PAUSE mode continues in excess of about eight minutes, the machine will automatically revert to the STOP mode.

Fig. 2-15 shows the circuit diagram. Fig. 2-16 shows the timing chart.

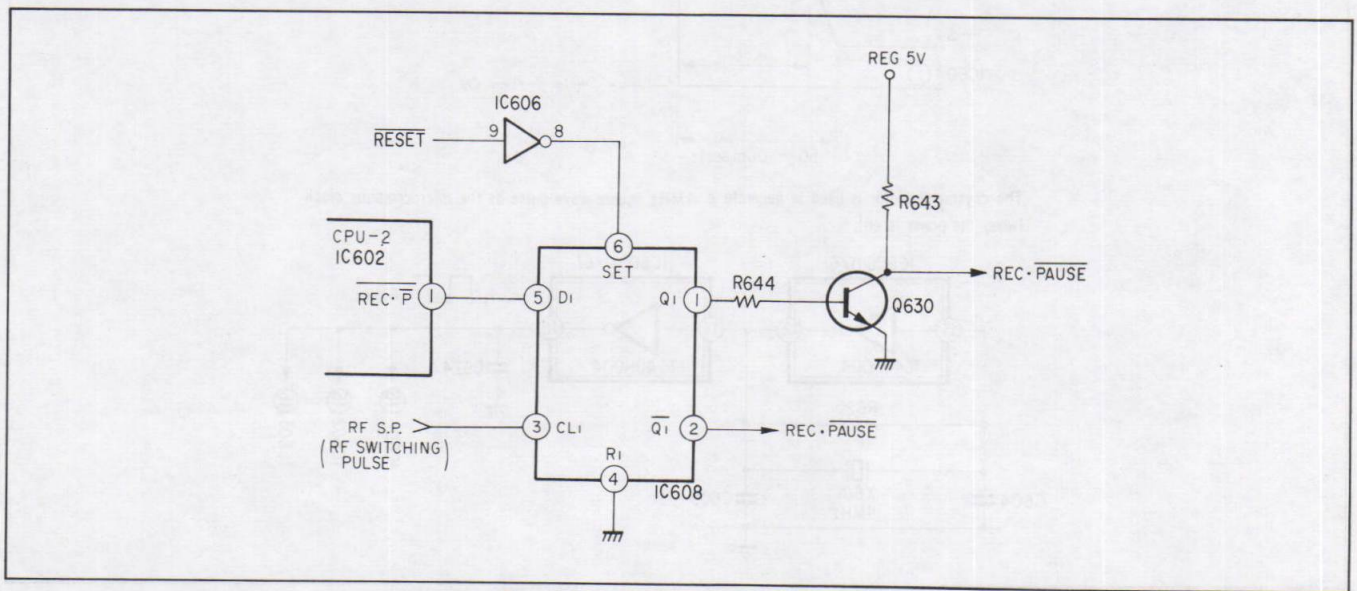


Fig. 2-15. Editing (TP) Circuit

In operation, a high signal output from pin 1 of CPU2 during REC + PAUSE is synchronized with an RF switching pulse by D-type flip-flop IC608, turning on Q630 and maintaining a REC + PAUSE state. The signal also synchronizes with an RF switching pulse when the REC + PAUSE state is released. This timing is shown in Fig. 2-16.

D-type flip-flop (IC608) is set (initialized) by applying a high signal to pin 6 while the power is on, reversing $\overline{\text{RESET}}$ by IC606.

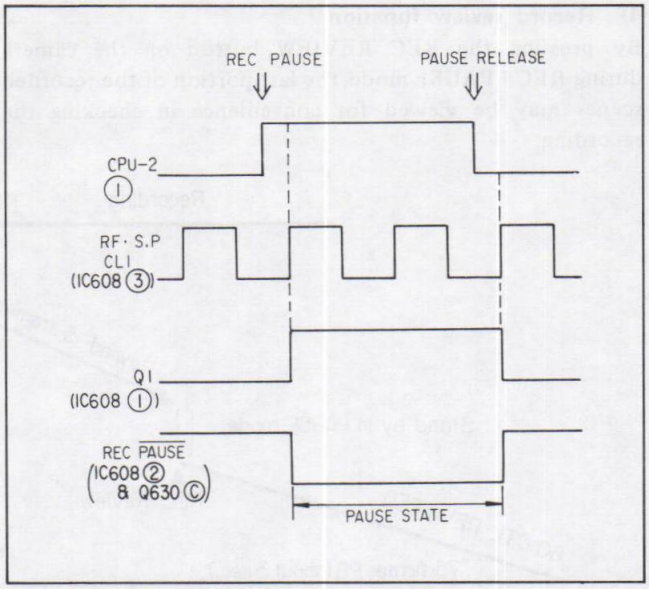


Fig. 2-16. Timing Chart

2-7-2. Power-on Reset and Clock Oscillator Circuit

The reset signal prevents a malfunction of the CPUs while the supply voltage rises when the power is turned on. The reset signal is generated by the circuit shown in Fig. 2-17.

In the circuit shown in Fig. 2-17, a voltage of 4.2V, obtained by voltage-dividing UNSWD 12V, is applied to pin 2 of comparator IC604, while pin 3 is the charge voltage for

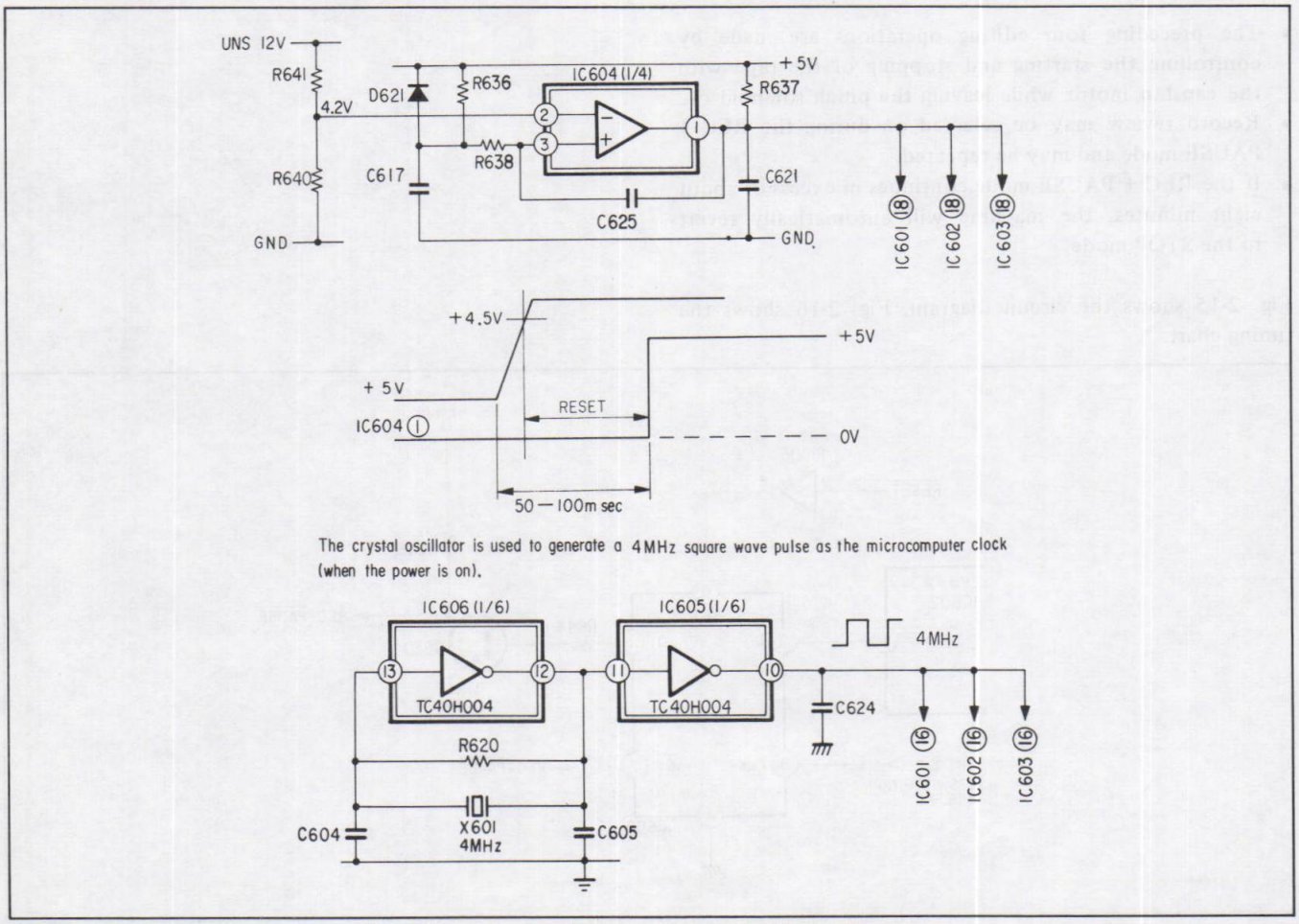


Fig. 2-17. Reset Circuit and Clock Oscillator Circuit

C617. Pin 1 remains low for about 100 ms after power is switched on, and a RESET signal is sent to the CPUs. The RESET signal is sent to CPU1, 2 and 3 and to the output expansion port of ICs 607 and 609.
To avoid a delay in the discharging of C617 and an absence of a reset signal when the power supply is repeatedly turned on and off, as well as chattering at the output of IC604 pin 1 positive feedback is applied to C625 discharge and to pin 3 of IC604.

2-7-3. Camera Control

Fig. 2-18 shows the camera control signal diagram.
System control signals used to control the camera are:

- CAMERA 12V (power for the camera)
- TALLY signal

Input signals to the system control from the camera are:

- CAMERA PAUSE
- REC REVIEW

Q602 and Q601 turn on by setting the input selection slide switch on the front section at the camera side, and 12V power will be supplied to the camera. The TALLY signal indicates that the VTR is running and lights an LED inside the view finder. The signal outputs is REC, PB, DUB, X2 and CUE/REV.

A high input to "CAMERA PAUSE" of pin 4 of CPU1 when the camera start/stop switch has been pressed. "Pause" and "Pause Release" operations are alternately performed each time this input is inserted.

By pressing the REC REVIEW switch on the camera, "R·REV" of pin 2 of the CPU1 goes high to start the REC REVIEW operation. The REC REVIEW operation plays the last portion of the recording (for 75 CTL pulses, about 3 seconds) for monitoring.

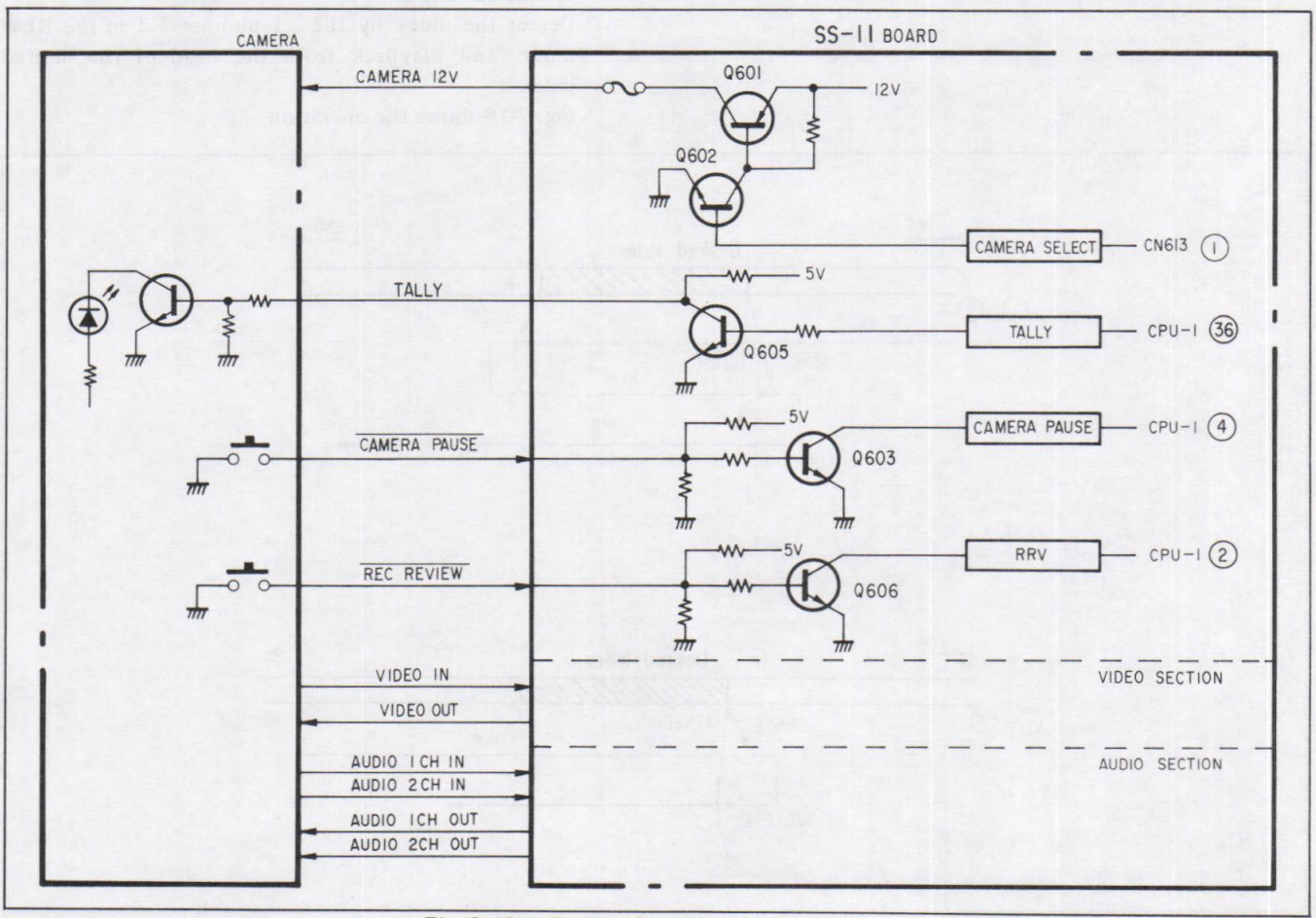


Fig. 2-18. Camera Control Signal Diagram

2-7-4. Index Write and Erase Circuit

There are two ways to write an index. IC603 (CPU3-3pin) output $\overline{\text{IND WRT}}$ turns "Low". The writing time is about 9 seconds.

1. Depress the APS MARK button in any position during PB.
2. Automatic write at start of Manual REC during the mode change of STOP→REC and STOP→REC + PAUSE→REC.
   (In index writing, CTL dury ratio changes from 50 to 20%.)

Erasing index

Search the address of the index to be erased by auto program search. When the VTR is searched and the mode becomes PB, press the APS ERASE button. By doing so, the VTR returns to the head of the index at x2 RVS speed, and the index is erased automatically.

IC603 (CPU3-4pin) output $\overline{\text{IND ERS}}$ goes low during erasing. The erasing time is about 15 seconds. (When erasing the index, change CTL dury ratio from 20% to 50%.) The APS display flashes during both writing and erasing. The rise and fall of the index WRT and ERS signals, which are output of IC603, are synchronized to the rise of INDEX CTL by the software.

2-7-5. Auto Program Search

The following three methods are possible for cuing and replay by the index:

1. After setting the program number by the APS key, press the PB key. (Absolute address search)

1) When the system control does not memorize the program number at the present position.
   Rewind to the tape top. Detect the index in the FF mode regarding the tape top as 1. When the desired index is detected, playback from the head of that index.

2) When the system control memorizes the program number at the present position.
   Determine if the desired index is before and after the present position. Detect it in the FF or REW mode, and playback from the head of that index.

2. After setting the program number by the APS key, press the FF key. (Relative address search in the forward direction)
   Detect the index by the set number in the FF mode, and playback from the head of the desired index.
3. After setting the program number by the APS key, press the REW key. (Relative address search in the reverse direction)
   Detect the index by the set number + 1 in the REW mode, and playback from the head of the desired index.
   Fig. 2-19 shows the operation.

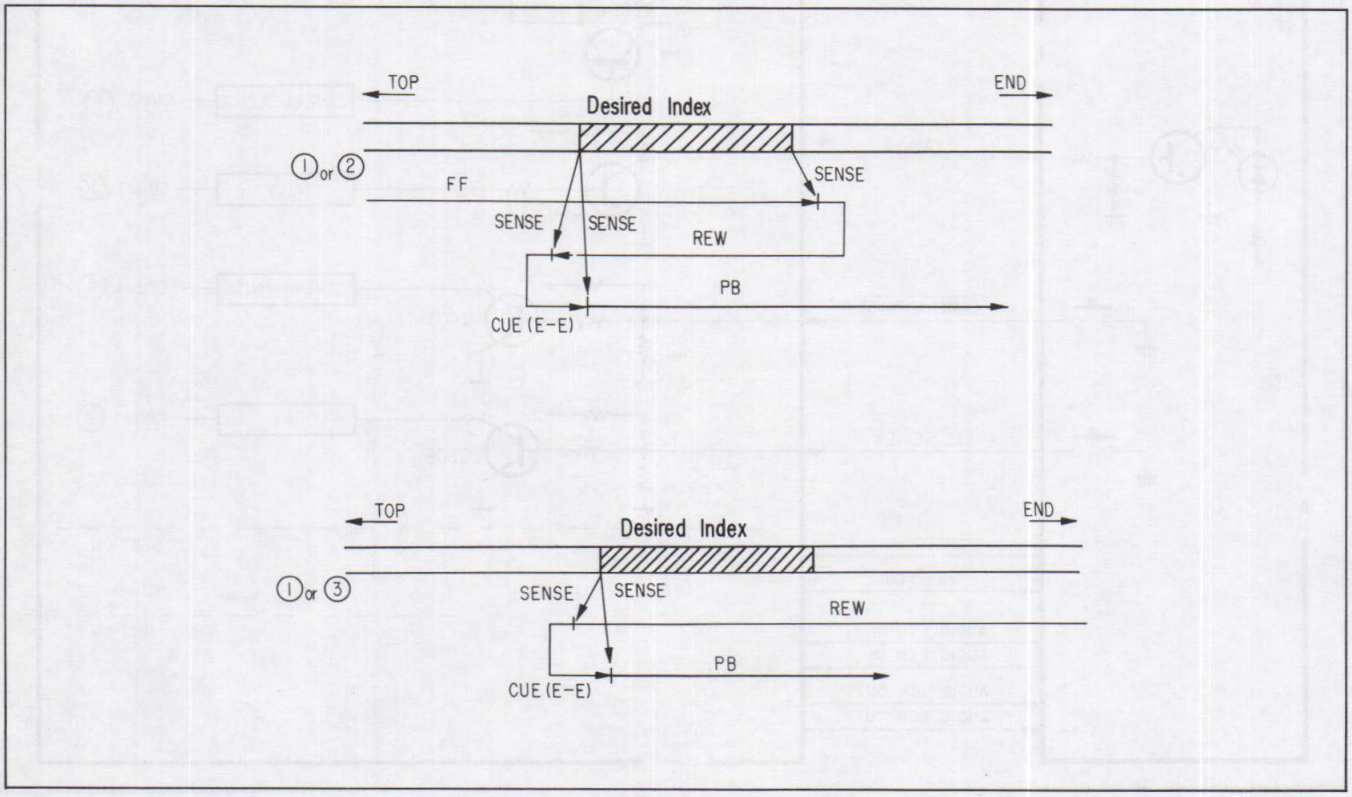


Fig. 2-19.

Index detection method

The hardware and the software are used to determine whether it is the index part or not according to the mode.

1. Detection by hardware
   The index sense circuit of 2-6-2 is used to detect the index. When the output of the index sense circuit is high in the FF/REW and the CUE/REV modes, the system control decides the index is there (The index CTL duty is 20%).

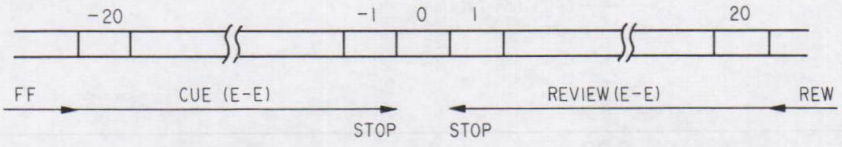
2. Detection by software
   The software is used to read whether the index CTL signal at pin 5 of IC603 is high or low. The index judgement is made by calculating the duty ratio.
   In the case of ±x1 and ±x2. (Since −x2 is one mode in index erasing, there is no function key corresponding to this mode.)

   Note: In modes other than the SLOW mode, the system control detects the index and memorizes the absolute address from the tape top.

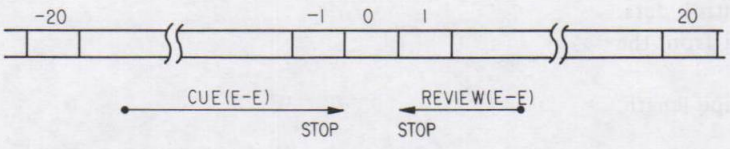
2-7-6. Memory Stop (GO TO ZERO)

The memory stop is a counter "0" stop and is performed by the GO TO ZERO button.
The memory stop button is effective only when the VTR is in the STOP mode. When memory stop is accepted, the VTR enters the REW or the FF mode according to the counter value. When the counter decreases to 0, the STOP mode sets in.
The memory stop performs 3 kinds of operation according to the absolute value of the counter value.

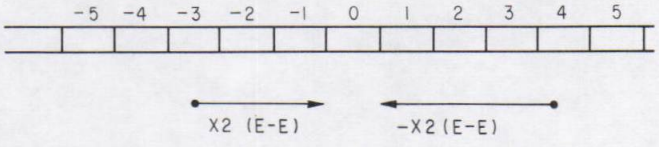
1. When $20 \leq |\text{counter value}|$



2. When $5 \leq |\text{counter value}| \leq 19$



3. When $|\text{counter value}| \leq 4$



2-7-7. Interface With External Control (For Changer) Terminal

The VTR deck has a connector for external equipment.

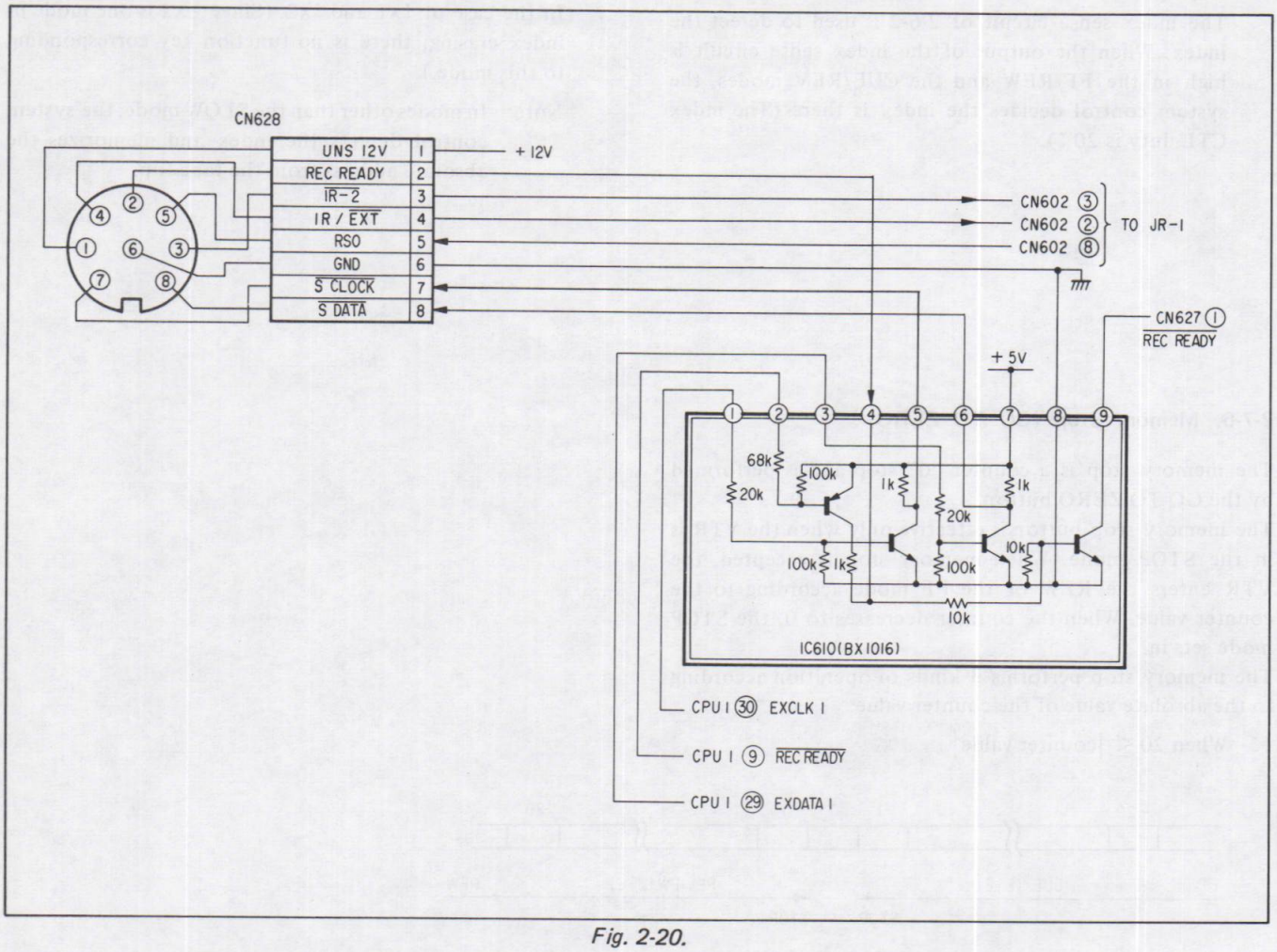


Fig. 2-20.

REC READY signal can determine the internal state from outside and the REC READY state can be set from outside. It is a common I/O port.

$\overline{\text{IR-2}}$ and IR/$\overline{\text{EXT}}$ are inputs for remote control data. $\overline{\text{S CLOCK}}$ and $\overline{\text{S DATA}}$ are reversed serial data from the expansion IC for CPU1 LED display.

RSO is the serial data to show the remaining tape length.

2-8. REMOTE CONTROL CIRCUIT

2-8-1. General

The remote control system is an infrared wireless remote control. The infrared signal from the commander is detected by D1 on the printed circuit board N in the photodetector block and is input to Pin 7 of IC001. The signal is amplified and filtered in IC001 and is output from Pin 1, to be input to two pins of CN201 on the printed circuit board JR-1 after passing through printed circuit board TU-24. The signal is designated as the IR signal.

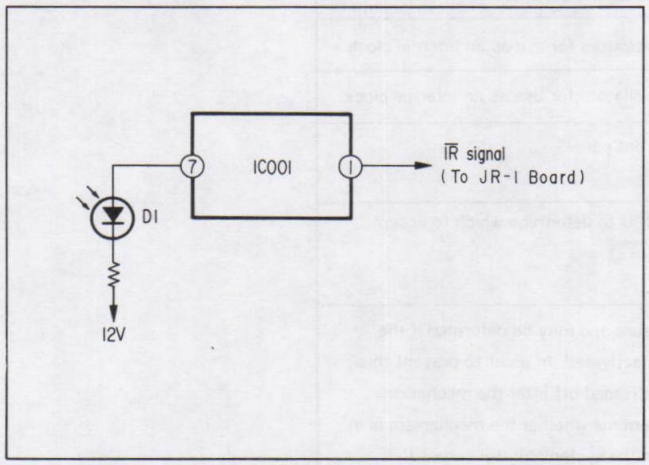


Fig. 2-21.

The IR signal is input to two pins of CN201 on printed circuit board JR-1, and the IR signal is input to one pin of IC201 after passing through Q201 and Q202. When both TV and VTR are connected by a multi-cable, the output of Q201 is also output to the TV side through the cable. Conversely, the output of the photodetector on the TV side is input to the base of Q202. Thus, both VTR and TV can be controlled by directing the commander to the photo-detector section of either TV or VTR.

2-8-2. Roles Played by Remote Control CPU (IC201)

- The input IR signal is output to the system control section as an SCO signal. The system controller decodes this signal and converts it into STOP, PB, REC, or other mode.
- CPU decodes the IR signal and outputs a pulse matching the selected channel to the tuner via the timer when direct tuning is performed by the commander.
- CPU can switch the power on or off. CPU decodes the $\overline{IR}$ or $\overline{PWR \cdot SW}$ signal, and the $\overline{PWR}$ signal is output from Pin 24 to the timer. The timer controls the power with this signal.

2-8-3. Functions of IC201

Pin No.	Designation	Function and Operation
1	$\overline{IR}$	Input signal from the photodetector section.
2	$\overline{IR2}$	Input signal from the changer in the same code as that of the $\overline{IR}$ signal.
3	$\overline{R \cdot P}$	$\overline{REC \cdot PAUSE}$ signal. Input signal from the system control section to prohibit tuner selection in the REC mode. L only during REC.
9	RST	RESET signal Power is supplied to the CPU by the POWER SW(MAIN SW). During that time, the RESET signal is input by Q205 for initialization.
11	OSC2	400kHz is generated by the ceramic osicllators for use as an internal clock.
12	OSC1	400kHz is generated by the ceramic osicllators for use as an internal clock.
15	$\overline{PWR\ SW}$	Input by ON/STANDBY switch on the front panel. The output is to Pin 24 .
16	$\overline{IR/EXT}$	The input signal from the changer for CPU to determine which to accept, commander input($\overline{IR}$), or changer input($\overline{IR2}$). L when changer input is accepted.
17	$\overline{STOP}$	The pinch roller, etc. remain under pressure and may be deformed if the power is cut off while the mechanism is activated. In order to prevent this, the CPU controls such that the power is turned off after the mechanism retracts. Therefore, the CPU hbs to determine whether the mechanism is in the stop status, or not. This signal frnm the system control serves this purpose. The signal is input via Q206 to match polarity and voltage level.
18	SWD 12V	The input signal which allows the CPU to determine whether power is being supplied or not, using the power which is turned on and off by the power switch on the front panel.
19	UK/$\overline{AEP}$	L : AEP model can select up to 30 channels H : UK model can select up to 12 channels
21	$\overline{UP}$	A pulse is output to move up a channel.
23	$\overline{RST}$	The output signal to reset the channel to the initial state(channel 1).
24	$\overline{PWR}$	Output to the power circuit via the timer circit to control L power.
25	$\overline{10}$	Output signals corresponding to keys 10 and 20.
26	$\overline{20}$	on the commander wher when performing direct tuning.

Table 2-13.

2-8-4. Signal Format

1) Input Signals ($\overline{IR}$ and $\overline{IR\text{-}2}$ Signals)

The input signal from the commander, or the changer, is a 10-bit signal with a duration of 28 ms per frame.

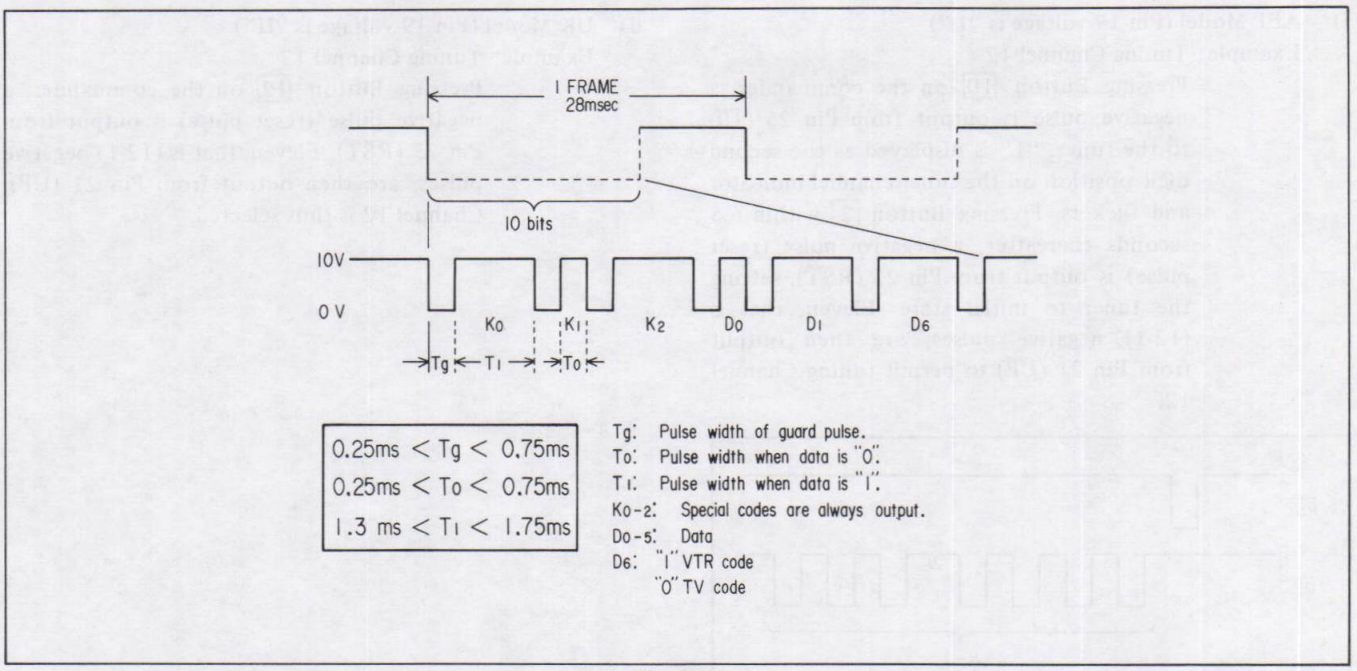


Fig. 2-22.

2) SCO Output Signal

The output signal to the system control section. One SCO output is made only when two successive pieces of input data are the same in order to minimize misoperation.

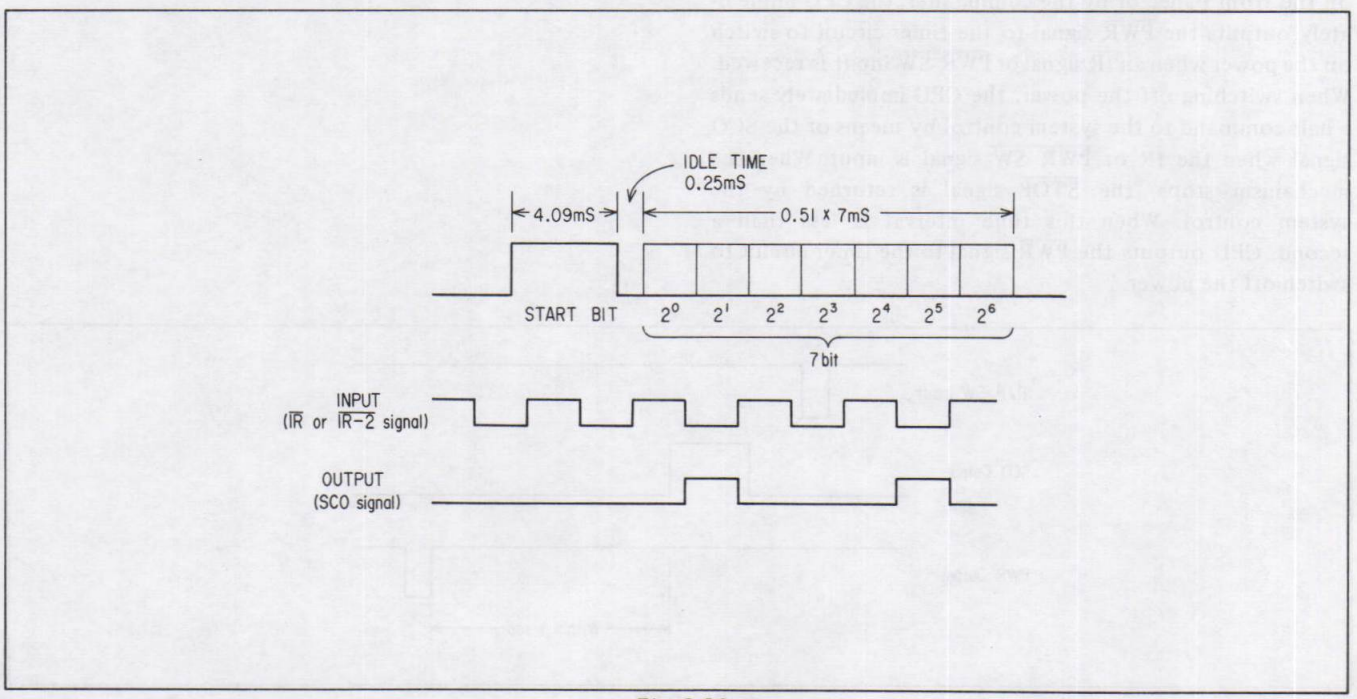


Fig. 2-23.

3) Tuning Output Signal

The equipment permits direct tuning using the commander. The numbers of channels that can be tuned differ between AEP and UK models, and the tuning methods are different. The tuning method can be changed by the voltage at Pin 19.

i) AEP Model (Pin 19 voltage is "L")

Example: Tuning Channel 12

Pressing Button [10] on the commander, a negative pulse is output from Pin 25 ($\overline{10}$) to the tuner. "1" is displayed as the second digit position on the tuner channel indicator and flickers. Pressing Button [2] within 6.5 seconds thereafter, a negative pulse (reset pulse) is output from Pin 23 ($\overline{RST}$), setting the tuner to initial state. Eleven, that is (12-1) negative pulses, are then output from Pin 21 ($\overline{UP}$) to permit tuning Channel 12.

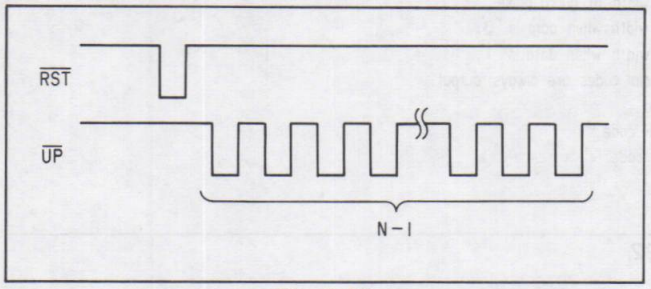


Fig. 2-24.

ii) UK Model (Pin 19 voltage is "H")

Example: Tuning Channel 12

Pressing Button [12] on the commander, a negative pulse (reset pulse) is output from Pin 23 ($\overline{RST}$). Eleven, that is (12-1) negative pulses, are then output from Pin 21 ($\overline{UP}$). Channel 12 is thus selected.

4) POWER ON/OFF Output Signal

When switching on the power by the ON/STANDBY switch on the front panel, or by the commander, the CPU immediately outputs the $\overline{PWR}$ signal to the timer circuit to switch on the power when an $\overline{IR}$ signal or $\overline{PWR\ SW}$ input is received. When switching off the power, the CPU immediately sends a halt command to the system control by means of the SCO signal when the $\overline{IR}$ or $\overline{PWR\ SW}$ signal is input. When the mechanism stops, the $\overline{STOP}$ signal is returned by the system control. When this time interval is less than a second, CPU outputs the $\overline{PWR}$ signal to the timer circuit to switch off the power.

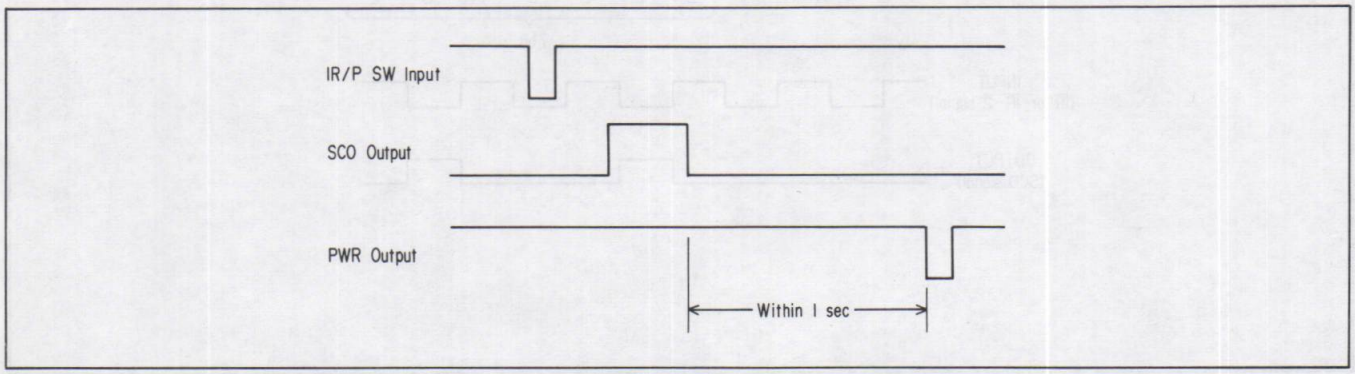


Fig. 2-25.

2-9. REMAINING TAPE INDICATOR CIRCUIT

2-9-1. General

The 4-bit microcomputer μPD652C040 contains a 1-kilobyte ROM (read-only memory). Programs are written in this ROM.

2-9-2. Function of IC501

Pin No.	Designation	Meaning	I/O	Function and Operation	Signal	
1	CL1	CLOCK 1	O	Clock output.	400KHz	
2	PC0	CAP LOCK	I/O	"H" when CAPSTAN SERVO is locked.		
3	PC1	CASSETTE IN	I/O	"H" when cassette threading is complete.		
4	PC2	PAUSE	I/O	"H" during PAUSE		
5	PC3	JOG	I/O	"H" during variable speed playback.		
6	PD0	REW	I/O	"H" during REW		
7	PD1	FF	I/O	"H" during FF		
8	PD2	RSO	I/O	Serial data out.		
9	PD3		I/O			Unassigned
10	PE0	LED 1	O	"H" when No.1 LED is displayed.		
11	PE1	LED 2	O	"H" when No.2 LED is displayed.		
12	PE2	LED 3	O	"H" when No.3 LED is displayed.		
13	PE3	LED 4	O	"H" when No.4 LED is displayed.		
14	Vcc	+5V	—			
15	TEST	TEST PORT	O			Unassigned
16	PF0	LED 5	O	"H" when No.5 LED is displayed.		
17	PF1	LED 6	O	"H" when No.6 LED is displayey.		
18	PF2	C CODE 0	O	Cassette codes are displayed in binary.		Unassigned
19	PF3	C CODE 1	O	Cassette codes are displayed in binary.		Unassigned
20	PG0	C CODE 2	O	Cassette codes are displayed in binary.		Unassigned
21	PA0	S · FG	I	S reel FG.	60 cycles/revolution	
22	PA1	T · FG	I	T reel FG.	60 cycles/revolution	
23	PA2	PB+DUB	I	"H" during PB or DUB.		
24	PA3	REC $\overline{\text{PAUSE}}$	I	"H" during REC.		
25	$\overline{\text{INT}}$	$\overline{\text{RTC}}$	I	Real Time Clock.	400Hz	
26	RES	RESET	I	Microcomputer reset signal.	"H" for several tens of msec when power is ON.	
27	Vss	OV(GND)	—			
28	CL0	CLOCK 0	I	Clock input	400KHz	

Table 2-14.

2-9-3. Operation

First, whether the tape is running at a constant speed is determined by detecting the mode signal from the system control circuit. The mode is discriminated as normal playback, record, or audio dubbing. When the tape is found to be running at a constant speed, the CAP LOCK signal determines whether or not the capstan servo circuit is phase-locked. When an unrecorded tape is played back, the capstan servo does not phase-lock (the CAP LOCK signal remains "L"), and no indication of the remaining tape is made. Next, the periods of the FG signal (S.FG signal) on the supply-side reel and of the FG signal (T.FG signal) on the tape-up side reel are measured by the RTC (real time clock) from the system control circuit. The type of cassette in use is determined by these two periods Ts and Tt, the remaining tape is calculated, and the six LEDs are sequentially illuminated to indicate the remaining tape quantity. The data showing the remaining tape quantity is converted into a serial signal (RSO signal) and is output to the changer terminal. Once the remaining tape quantity is calculated, it continues to be calculated and displayed no matter in what mode the system is set.

A description of determination of cassette type and calculation of remaining tape quantity is given in the following. Assuming the periods of the FG signal (S.FG) of the supply reel to be Ts and of the FG signal (T.FG) of the take-up reel to be Tt, both Ts and Tt have a relationship that can be expressed by the following equation:

$$Ts^2 + Tt^2 = (K \cdot \sqrt{R0^2 + R1^2})^2$$

where R0: reel diameter
R1: winding diameter when all tape is wound on the reel
K : constant

The calculations will produce a circle with a radius of $K \cdot \sqrt{R0^2 + R1^2}$ centering on the origin. Both R0 and R1 differ depending on the cassette type, and six types of concentric circles can be obtained. Tt at the tape top and Ts at the tape end are determined by the reel diameter and will be the same value.

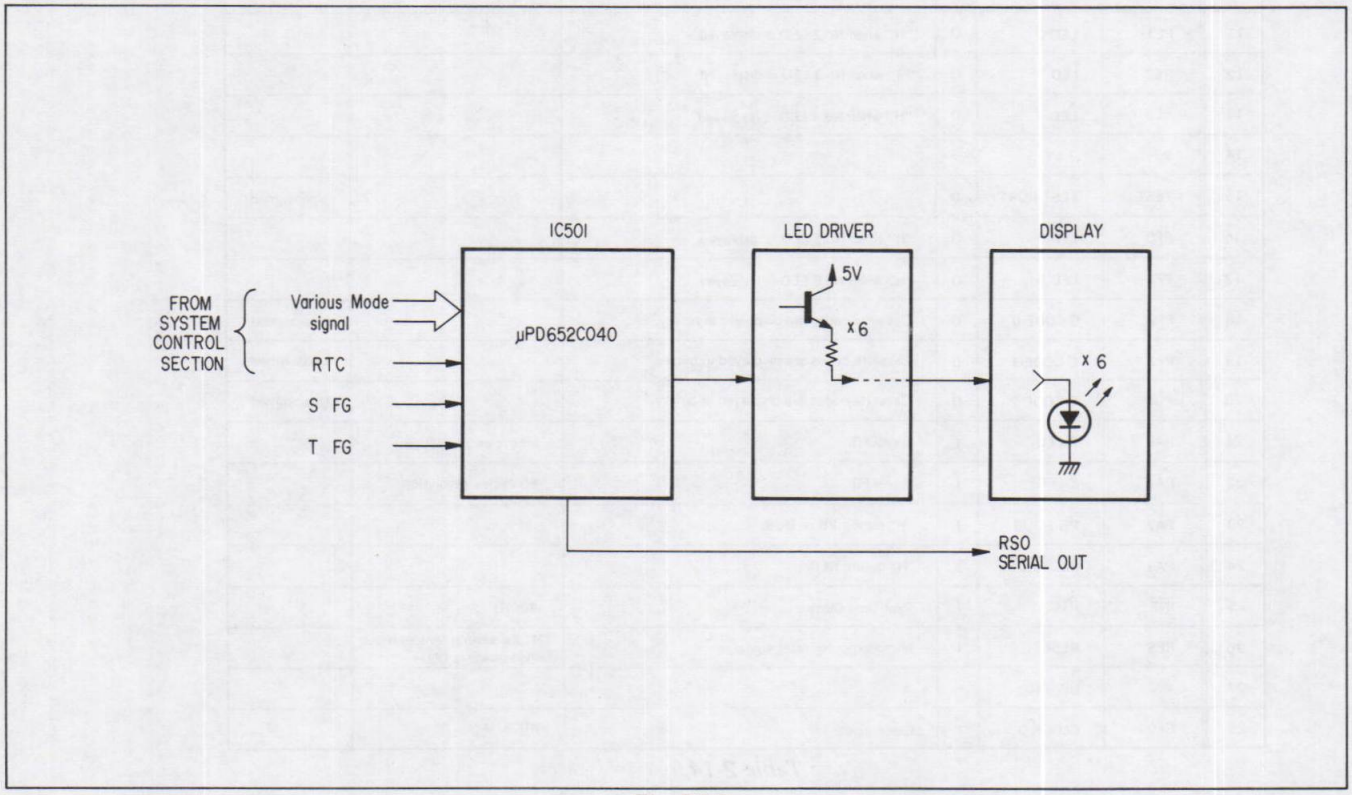


Fig. 2-26.

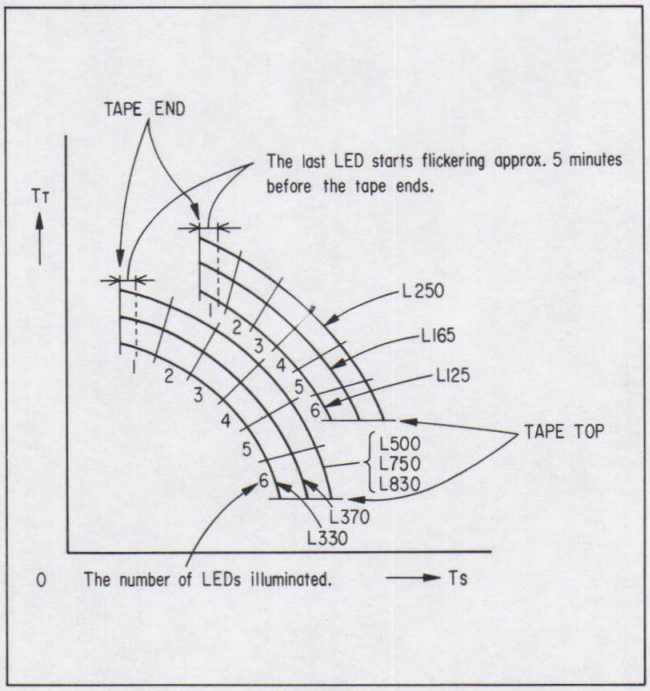


Fig. 2-27.

As Figure 2-27 indicates, the cassettes are grouped into two groups-those from L125 to L250 with a thicker reel diameter and those from L330 to L830 with a thinner reel diameter. L500, L750, and L830 have equal R0 and R1 and positions on the same curve.

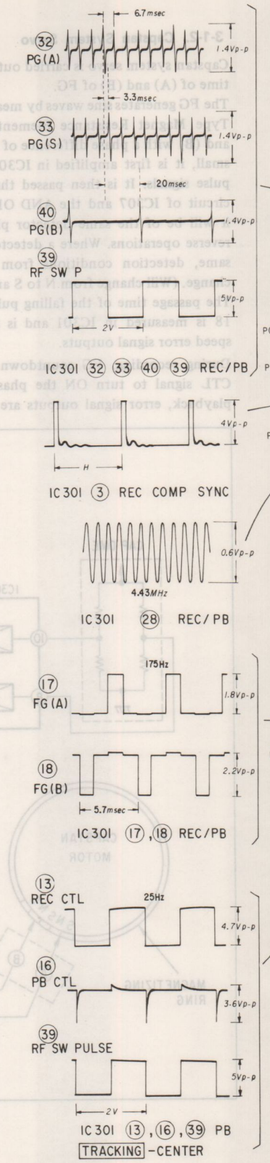
The microcomputer determines the cassette type by the position of the points (Ts and Tт) that are determined by the period Ts of the supply reel FG and Tт of the take-up reel FG during running at a constant speed. Specifically, the cassette type is determined by on which of the six curves these points (Ts and Tт) are positioned. Next, the ratio between Tт and Ts is calculated, and a determination is made as to in which parts of the curve, divided into six equal sections the points (Ts and Tт) position. The remaining tape quantity is then indicated. The last LED is flashed approximately 5 minutes before the tape end to indicate that the tape end is approaching.

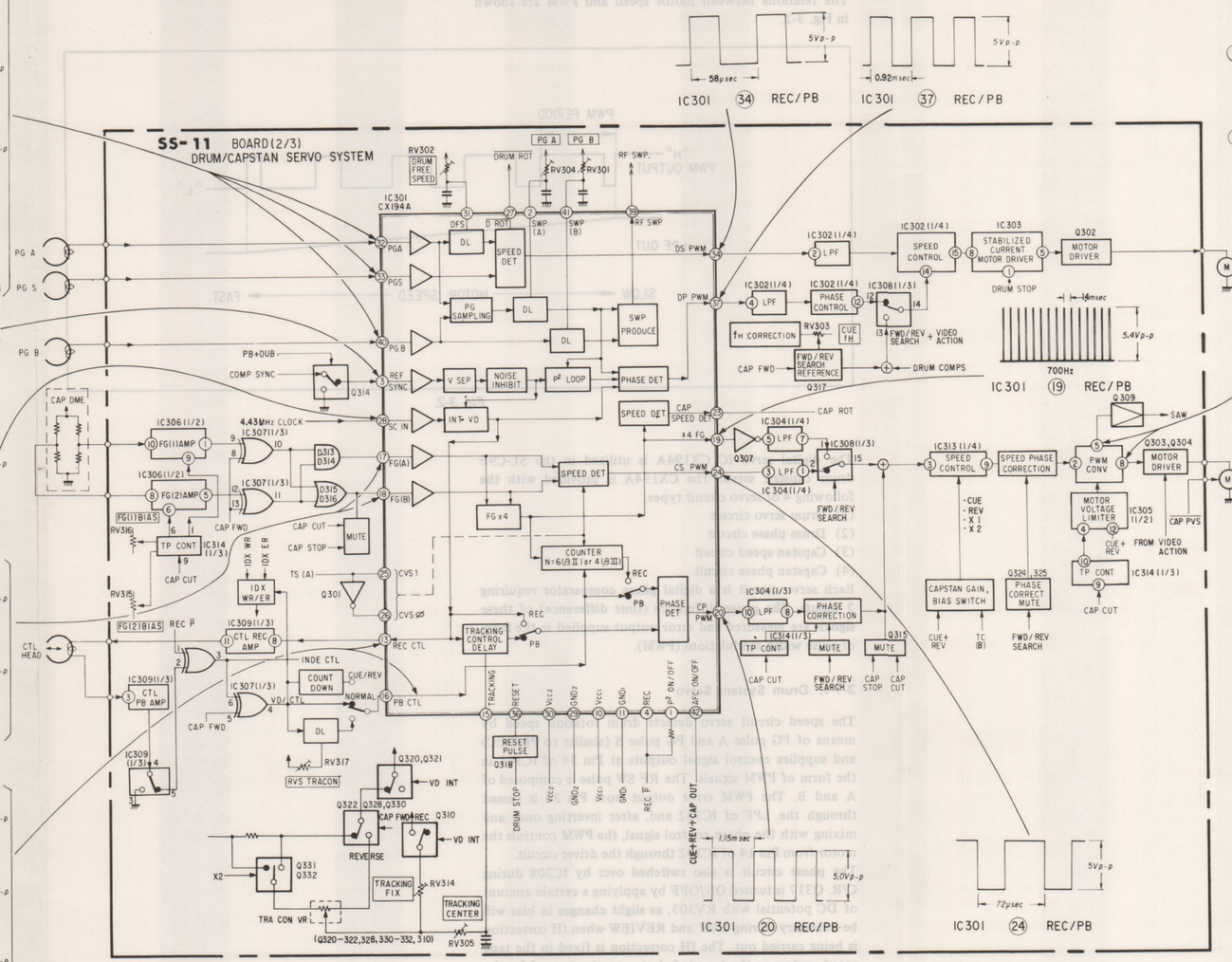
SECTION 3
SERVO CIRCUIT

Introduction

The servo circuits are located on the SS-11 and JR-1 Boards. The servo system is divided into three sections: main servo, and variable-speed servo.

The main servo consists of the drum-speed system, drum-phase system, capstan-speed system, and capstan-phase system. All four system are contained within a digital servo IC, CX194A. In addition to the drum-servo and capstan-servo systems, the main servo also includes the CTL and TRACON (tracking controls) systems. See Fig. 3-1.





SIGNALS	LOGICSTATE
CAP. FWD	NOMAL FWD "H", PVS "L"
DRUM. STOP	DRUM. STOP "H", DURING ROTATION "L"
CAP. STOP	CAP. M. STOP "H", DURING ROTATION "L"
FWD / REV SEARCH	C/R "H"
VD INT	REC. STOP. REC.P "L", PB "H"
CAP. ROT	STOP "L", DURING ROTATION "H"
DRUM. ROT	STOP "H", DURING ROTATION "L"
TAPE SPEED	A: X2 H, X1 L; B: L, H
CONPO. SYNC	ONLY WHEN VIDEO INPUT (V.H.SYNC)
CAP. CUT	PB-PAUSE REC-PAUSE SWING SEARCH "H" "L" OTHER MODES "L"
STEP. RVS	CONTROL OF CAP MOTOR FWD AND RVS
MOTOR TERMINAL	FWD "H" (CAP. SERVO "H") RVS "L" (CAP. SERVO "H")
STEP FWD	FRAME-BY-FRAME "H"

Fig. 3-1. Servo System Block Diagram

3-1. MAIN SERVO

The relations between motor speed and PWM are shown in Fig. 3-2.

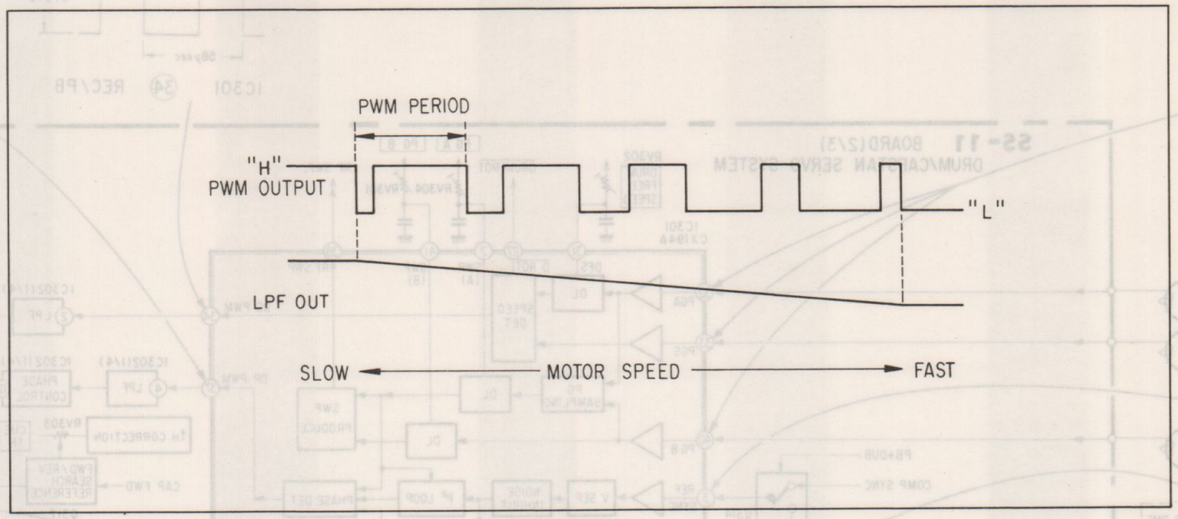


Fig. 3-2.

The digital servo IC CX194A is utilized in the SL-C9E drum capstan servo. The CX194A is provided with the following 4 of servo circuit types.

(1) Drum servo circuit
(2) Drum phase circuit
(3) Capstan speed circuit
(4) Capstan phase circuit

Each servo circuit is a digital phase comparator requiring 2 inputs. The phase difference (time difference) of these signals are measured and error output supplied in the form of pulse width modulations (PWM).

3-1-1. Drum System Servo

The speed circuit servo detects drum rotation speed by means of PG pulse A and PG pulse S (similar to PB/REC) and supplies control signal outputs at Pin 34 of IC301 in the form of PWM signals. The RF SW pulse is composed of A and B. The PWM error output from Pin 34 is passed through the LPF of IC302 and, after inverting once and mixing with the phase control signal, the PWM controls the motor from Pin 14 of IC302 through the driver circuit.

The phase circuit is also switched over by IC308 during C/R. Q317 is turned ON/OFF by applying a certain amount of DC potential with RV303, as slight changes in bias will be necessary during CUE and REVIEW when fH correction is being carried out. The fH correction is fixed in the tape speed system as the tape is fed at a constant speed by the capstan. In addition, DRUM STOP signals are fed to Pin 1 of IC303.

3-1-2. Capstan System Servo

Capstan system servo is carried out by detecting the passage time of (A) and (B) of FG.

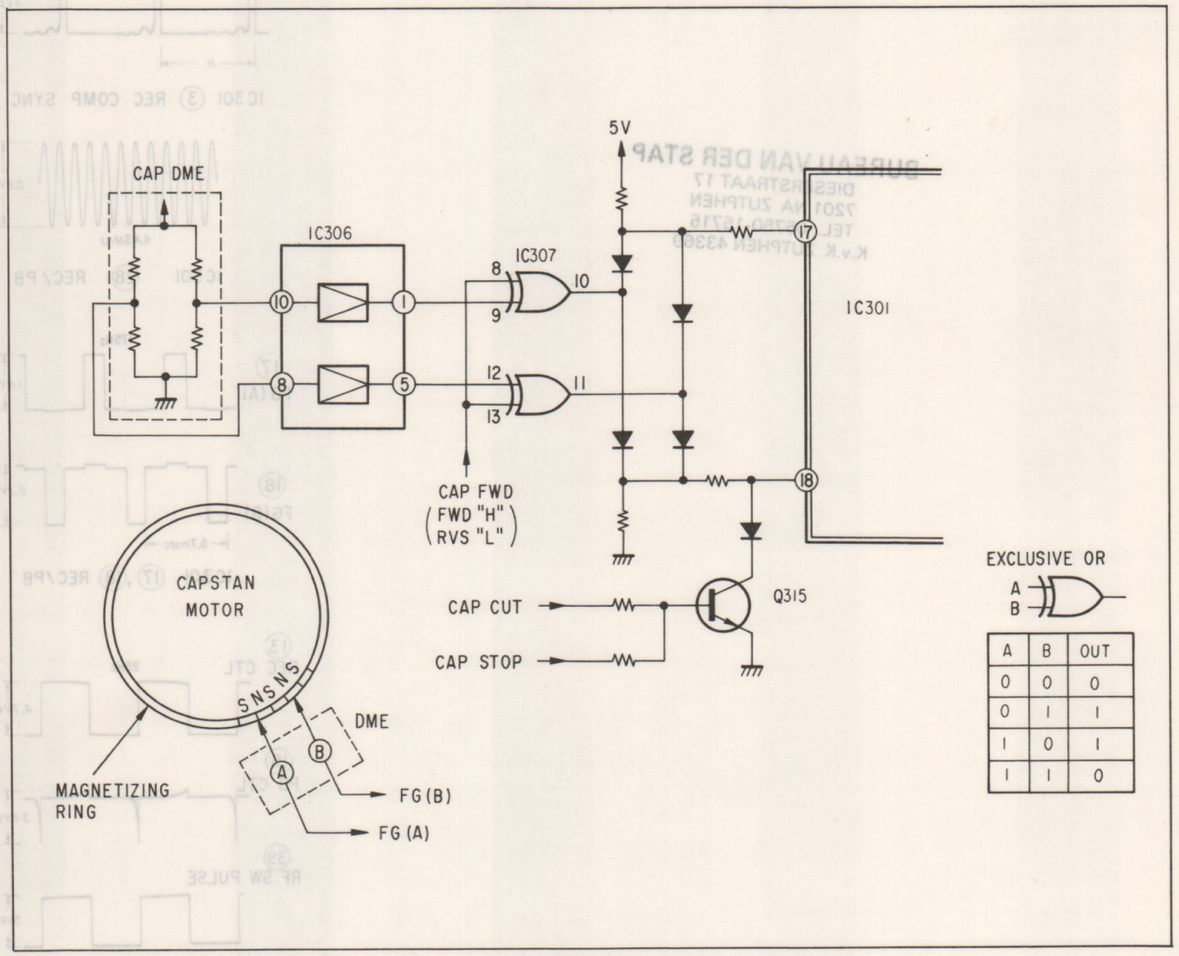
The FG generates sine waves by means of the DME (Dividing Type Magnet Resistance Element) and provides FG (A) and (B) with a phase difference of 90°. As the FG output is small, it is first amplified in IC306 and then converted to pulse signals. It is then passed through the Exclusive OR circuit of IC307 and the AND OR circuit of the diode so it will be of the same detector phase during forward and reverse operations. Where a detector phase is not made the same, detection conditions from the DME will tend to change. (Will change from N to S and S to N).

The passage time of the falling pulses entering Pins 17 and 18 is measured in IC301 and is supplied in the form of speed error signal outputs.

During recording, FG countdown is used in place of the CTL signal to turn ON the phase system servo. During playback, error signal outputs are supplied in the form of PWM signals by phase detection using the CTL signals entering Pin 16. The error PWM signals obtained from IC301 are fed to the OP amplifier after passing through the LPF of IC304 and mixing with the speed system. One side of the OP amp (negative) is changed over in each mode or 4 circuits (CUE, REVIEW, X1, X2) to determine the respective bias and gain.

To improve on the efficiency of the power supply, the output of IC304 is converted to PWM signals in IC305 and sent to the motor as DC output, after passing through the LPF once more.

The TL494CN is provided with an oscillation output of about 65 kHz. This oscillator output is a sawtooth wave of 0 to 3V and is impressed on the negative side of the comparator. The error voltage is changed to PWM signals by impressing it on the positive side and is supplied as output to the motor drive stage and controls the capstan motor after passing through the LPF.



A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

Fig. 3-3.

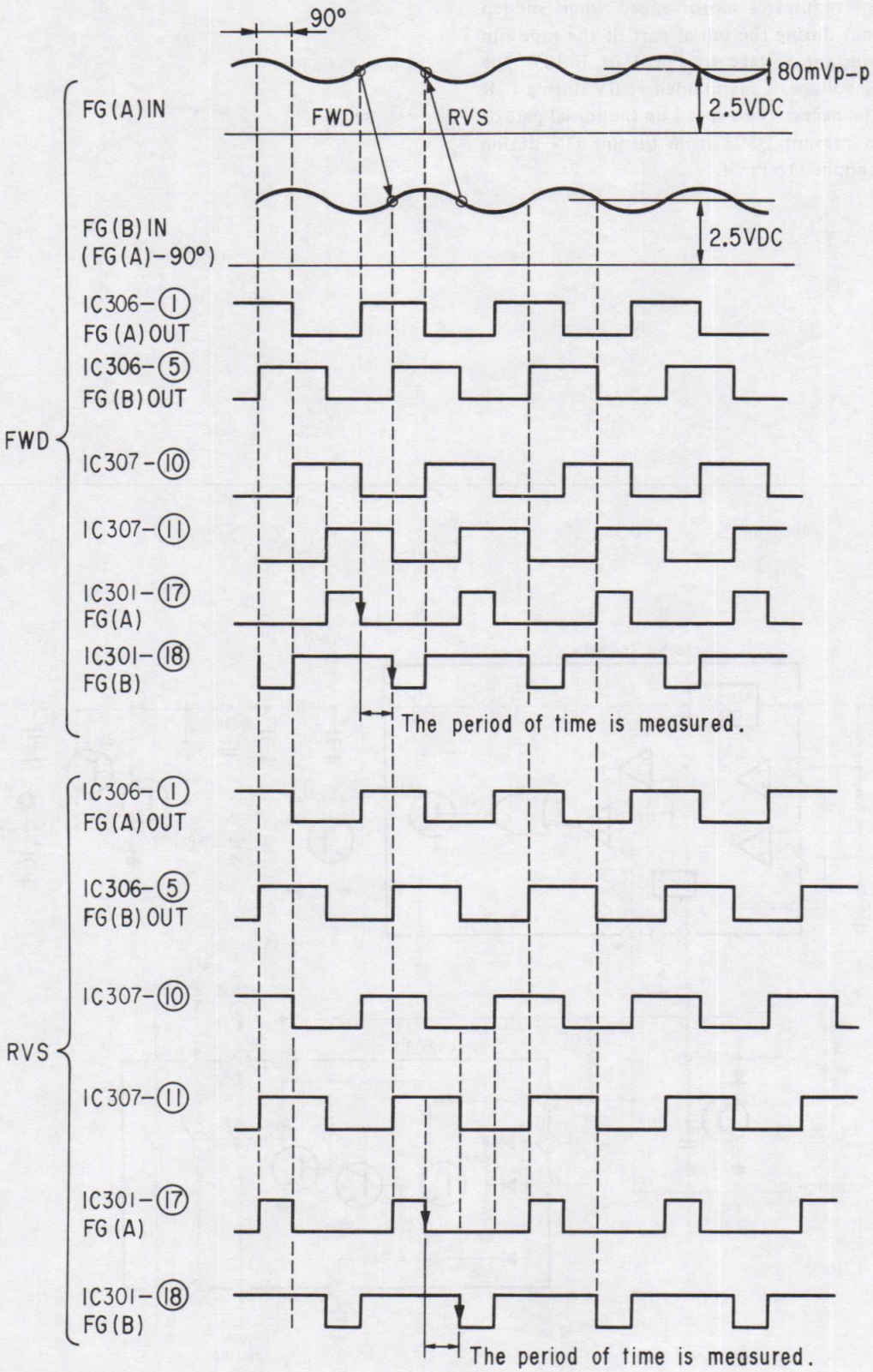


Fig. 3-4. FG Signal Timing Chart

3-1-3. Dead-time Control

Dead-time control suppresses motor speed when sudden voltage surges occur during the initial part of the tape run by applying a constant voltage to Pin 4 of IC305. The dead-time control voltage is maintained at 0V during C/R and TP as it will be necessary to speed up the initial part of the tape run. To prevent Q303 from turning ON during CAP STOP, 5V is applied to Pin 4.

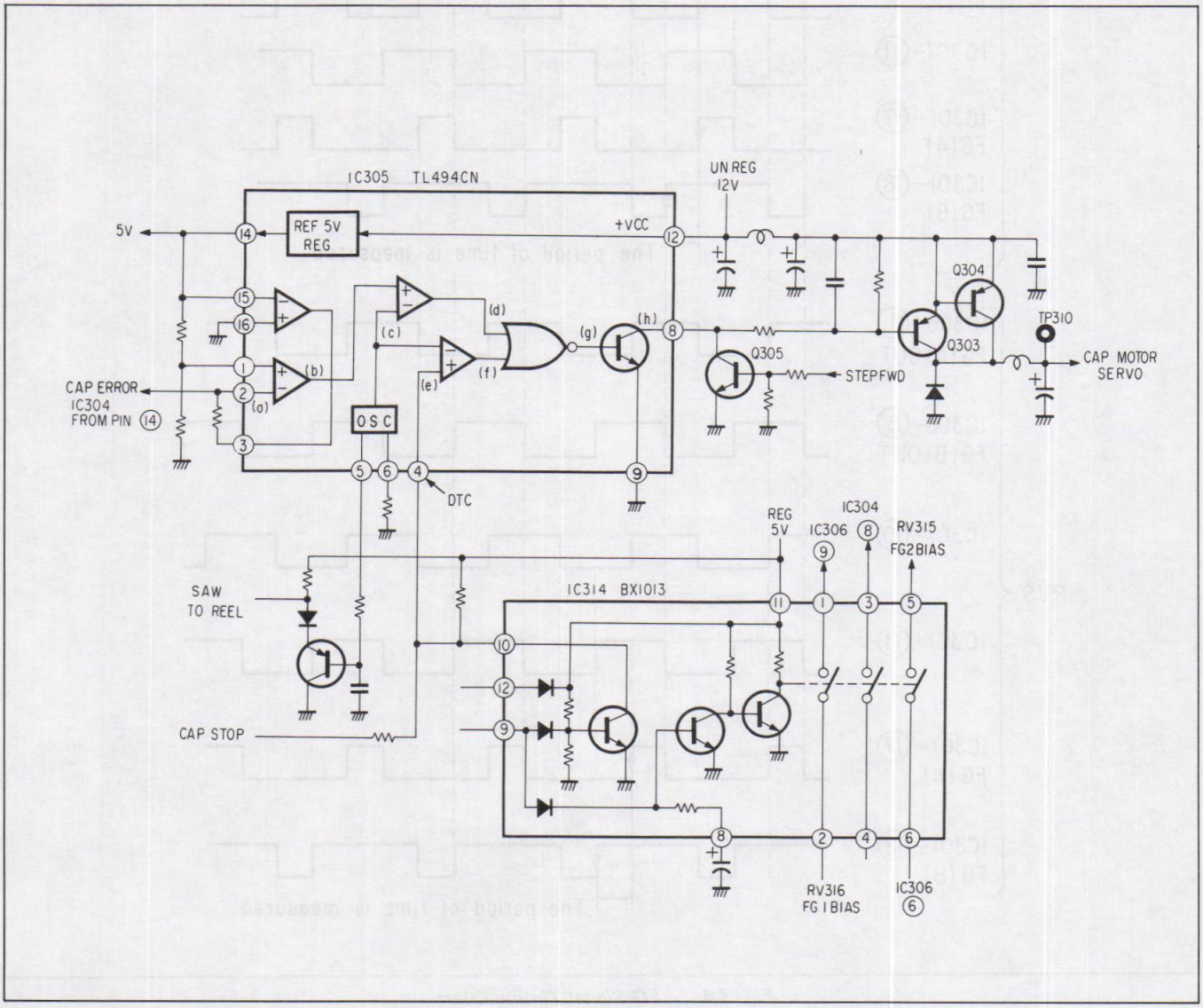


Fig. 3-5.

Dead-time control terminal (D.T.C.) Pin 4 of IC305

	IC 305 – ④	CAP MOTOR
NORMALLY	1.8V	5V
SPEED SEARCH	0 V	12V
CAP STOP	5 V	0V

Sets MAX DUTY to 90% during C/R and enables smooth rotation of motor during C/R release.

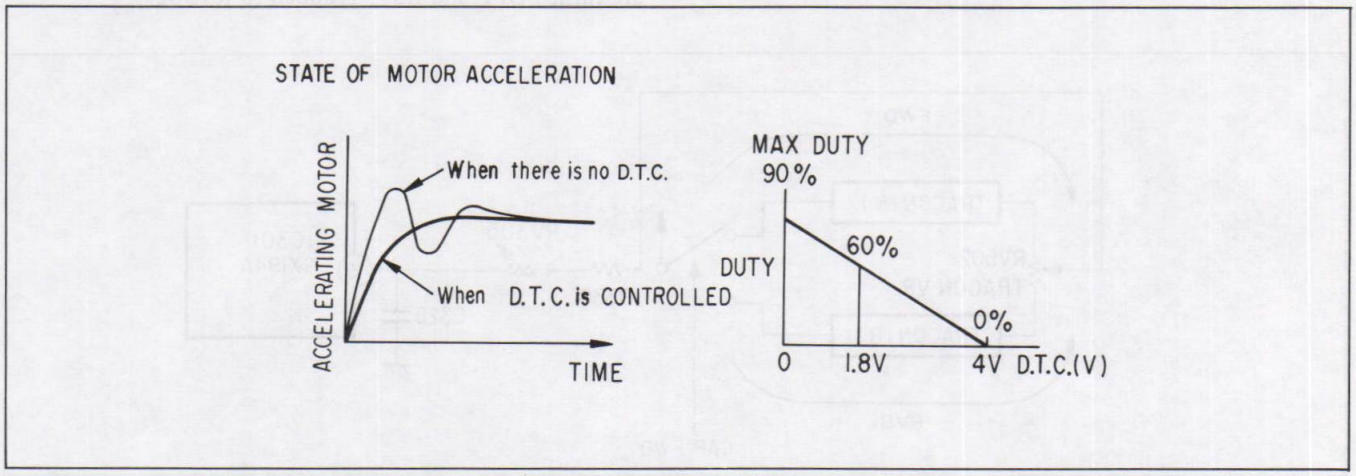


Fig. 3-6.

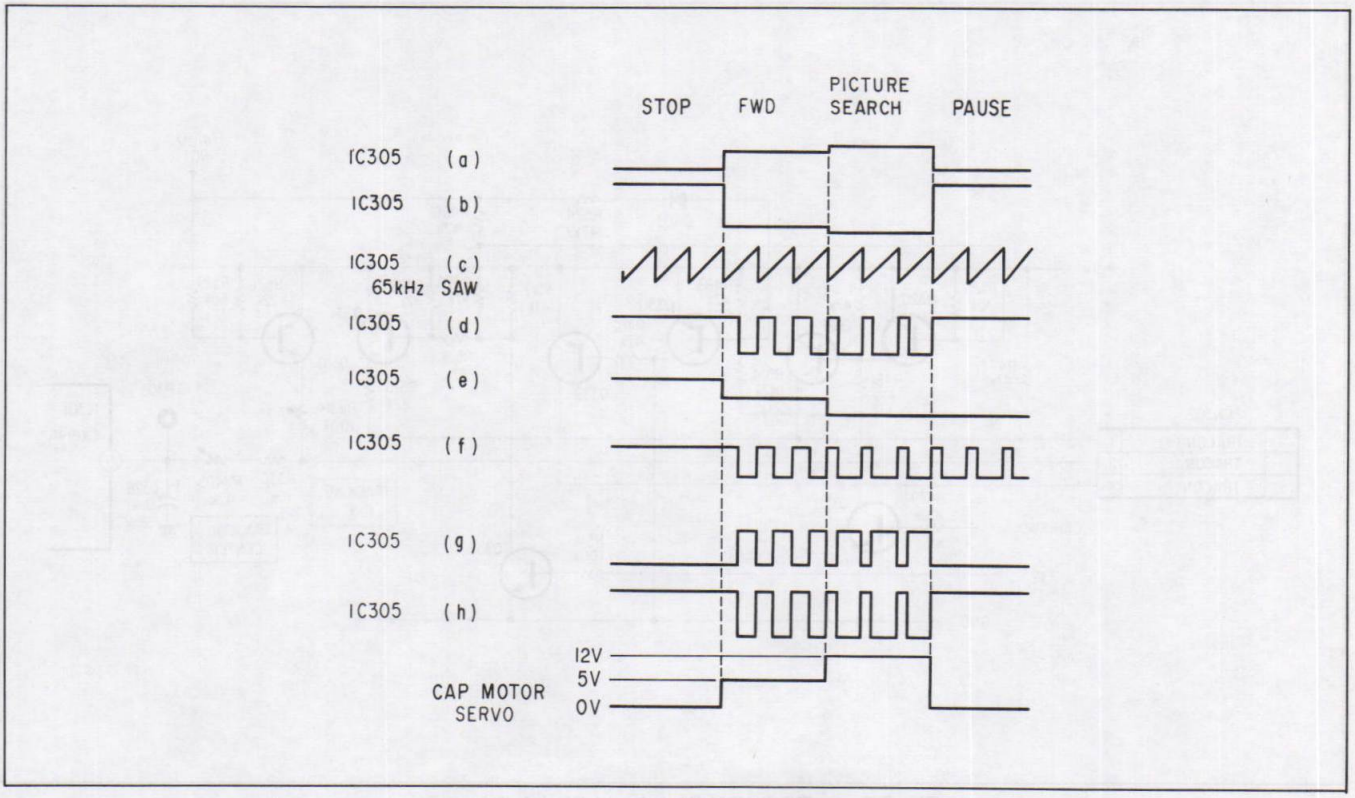


Fig. 3-7.

3-1-4. Servo During C/R

Although the servo is also operated by the capstan during C/R, 4 x FG output, used as an output voltage, is too low to drive in its original state.

As the capsatn will travel in direction "H" when speed is increased, the signal is inverted in Q307 to cause it to move in direction "L" and then acts to detect the speed after passing through the LPF. This signal is switched over in LC308 during C/R and applies a speed error signal to IC304.

3-1-5. TRACON Circuit

The peripheral circuits of TRACON are shown in Fig. 3-8 and 3-9.

TRACON becomes necessary as there is some phase difference in Normal PB, CUE, REV., X1, X2, −X1 and TP. TRACON is carried out during normal FWD by changing the multiduties of Pin 15 by means of RV502 (FU-5 Board), RV305 and C328. The opposite side of RV502 is used during RVS.

TRACON during X2

Q328 and Q331 are turned ON during X2, Q332, and Q321 are turned OFF and R515 is added to RV502.

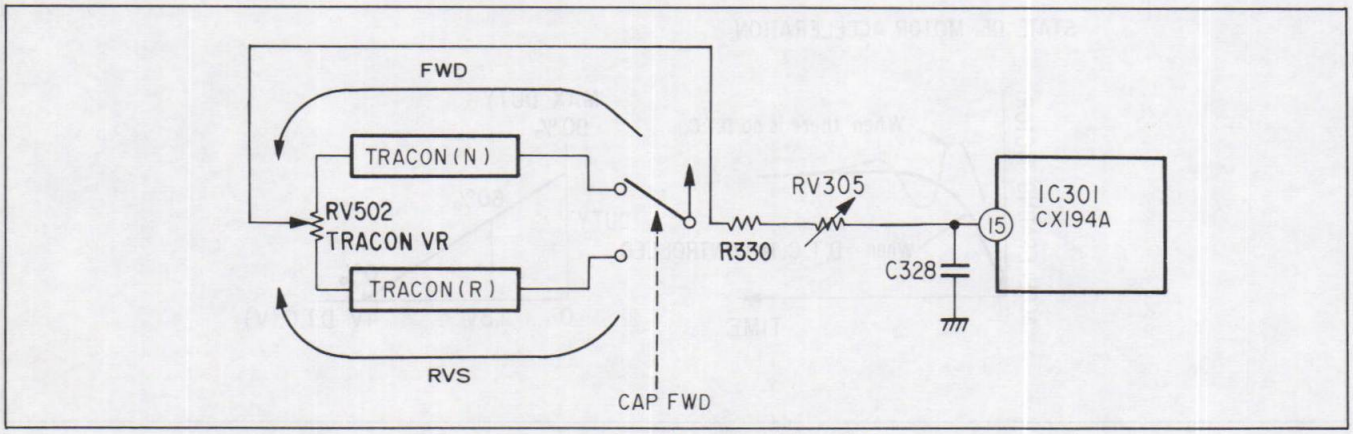


Fig. 3-8. TRACON Peripheral Circuit Diagrams

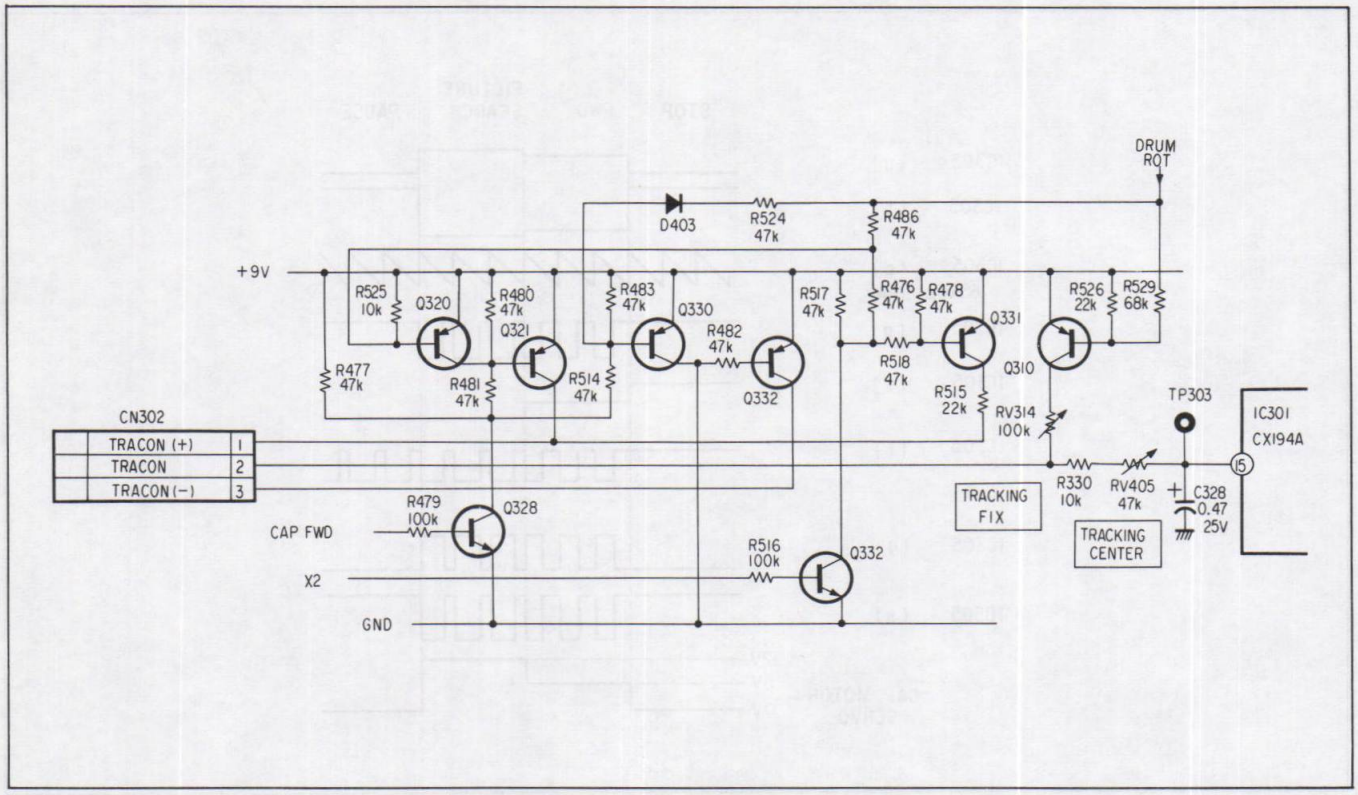


Fig. 3-9. TRACON Peripheral Circuit Diagrams

3-1-6. Timing Chart

The speed of the respective drum and capstan will now be discussed; the reference signal of the phase system and the time chart.

1) Drum speed system

PG A, PGs (REC/PB)

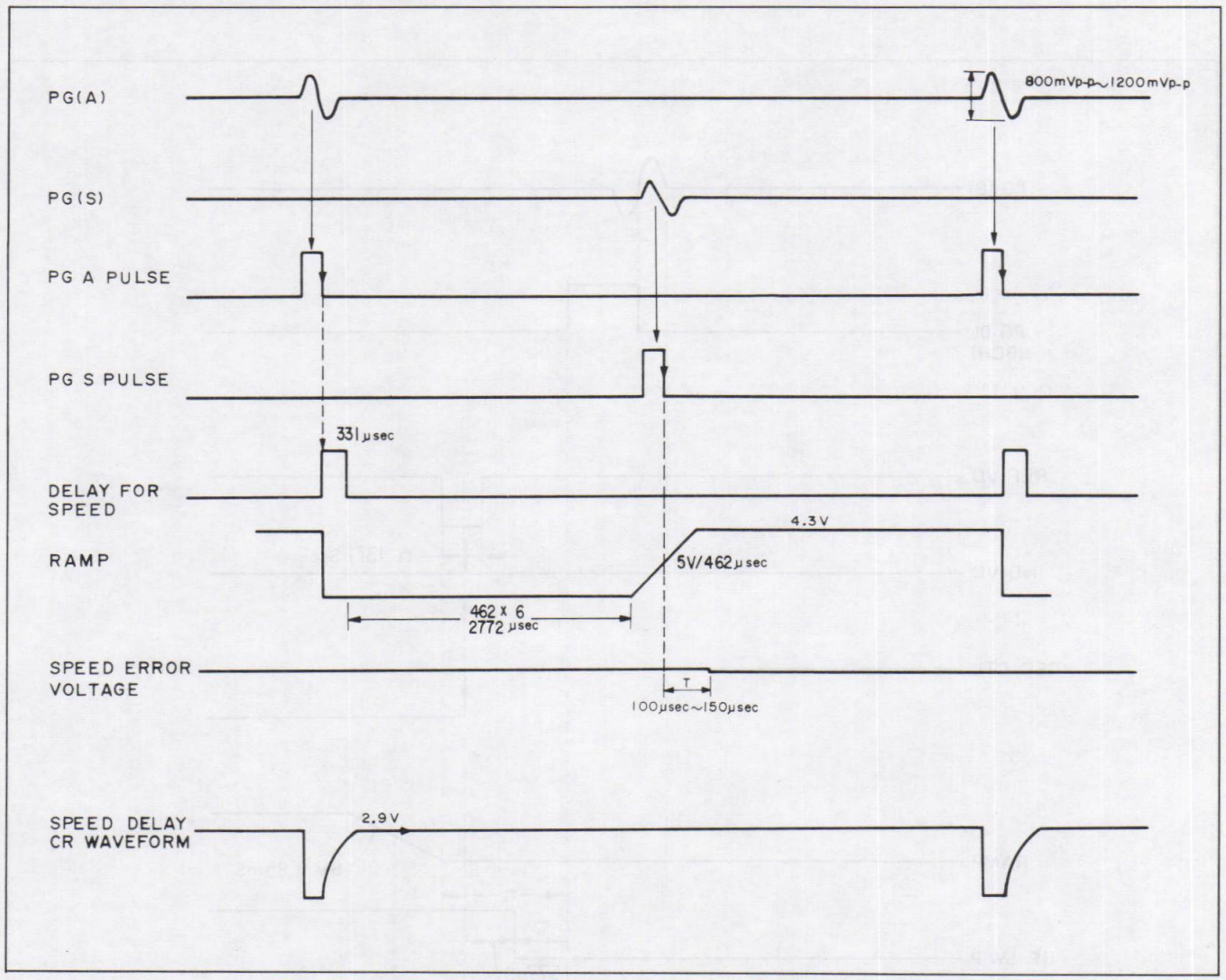


Fig. 3-10. Drum Speed System Timing Chart

2) Drum phase system

MODE	SERVO CONTROL SIGNAL	REFERENCE
REC	PG B	VD
PB	PG B	INT VD

VD : V Syncronism of Video Signal

INT.VD : VD from the internal X'tal

Table 3-1. Drum Phase System

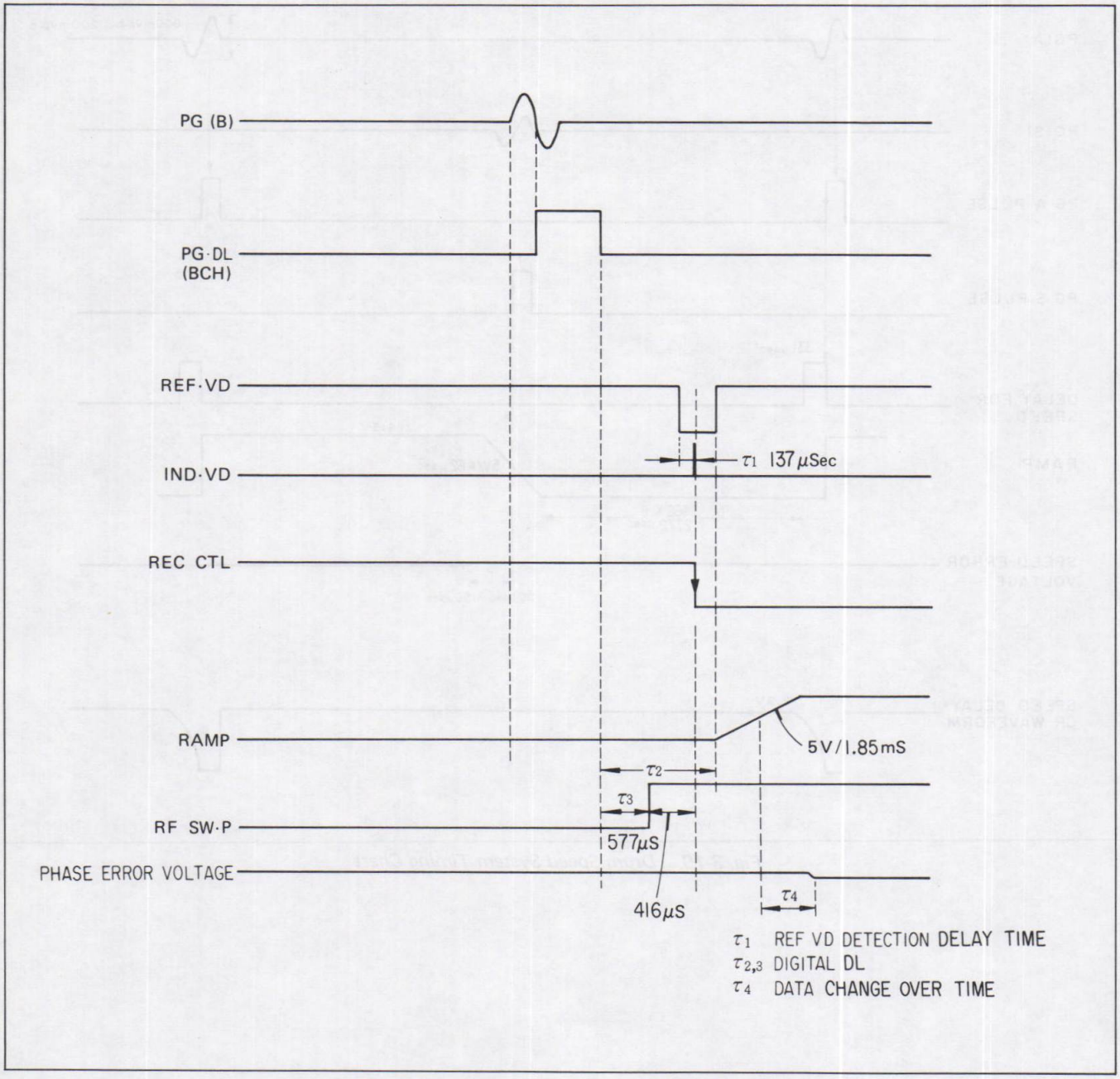


Fig. 3-11. Drum Phase System Timing Chart

3) Capstan phase system

MODE	SERVO CONTROL SIGNAL	REFERENCE
REC	CAP.FG 25Hz	VD
PB	CTL	TRACON MONO-MULTI OUTPUT + INT VD

Table 3-2. Capstan Phase System

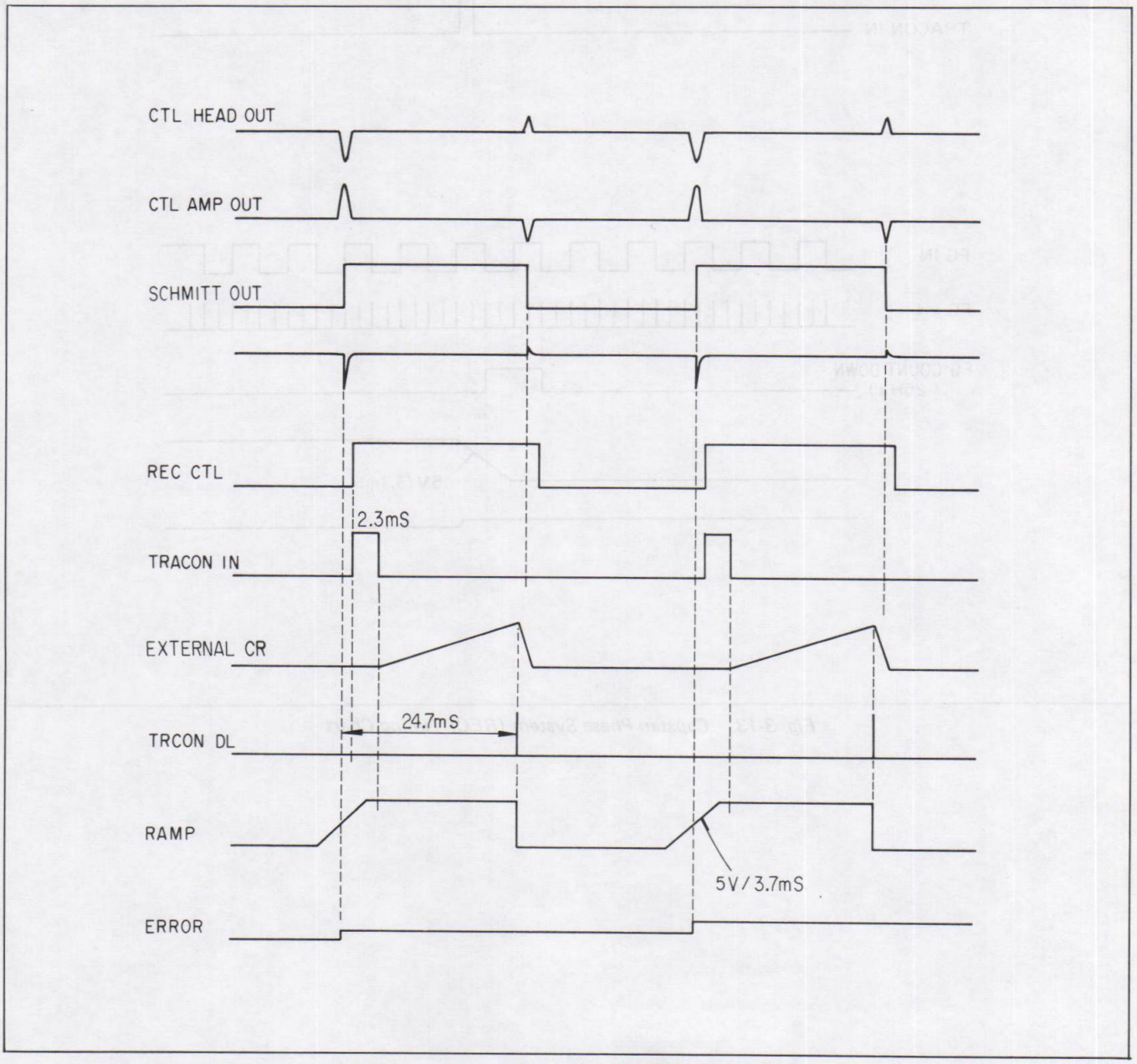


Fig. 3-12. Capstan Phase System (PB) Timing Chart

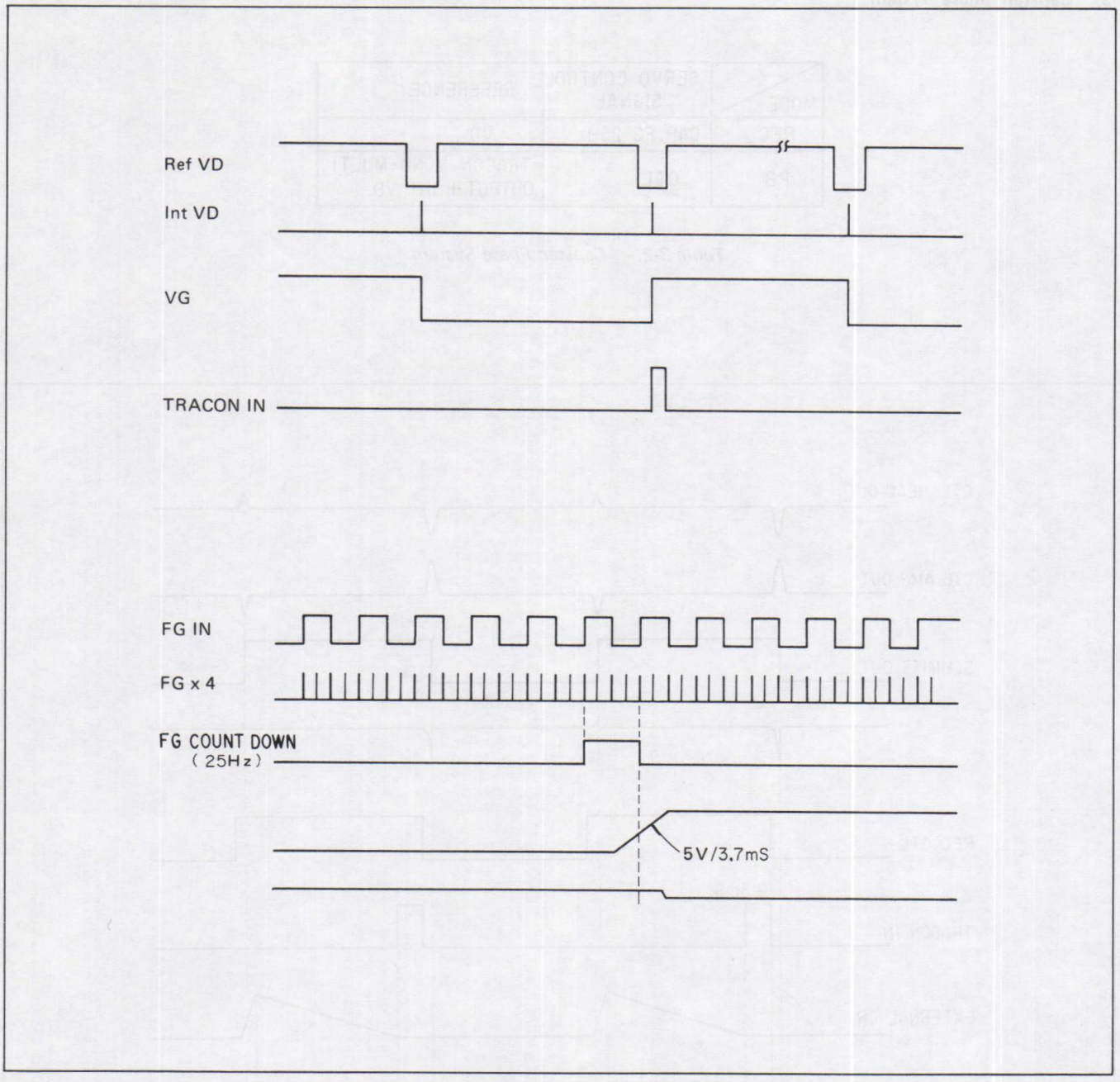


Fig. 3-13. Capstan Phase System (REC) Timing Chart

4) Capstan speed system

REC/PB FG(A), FG(B)

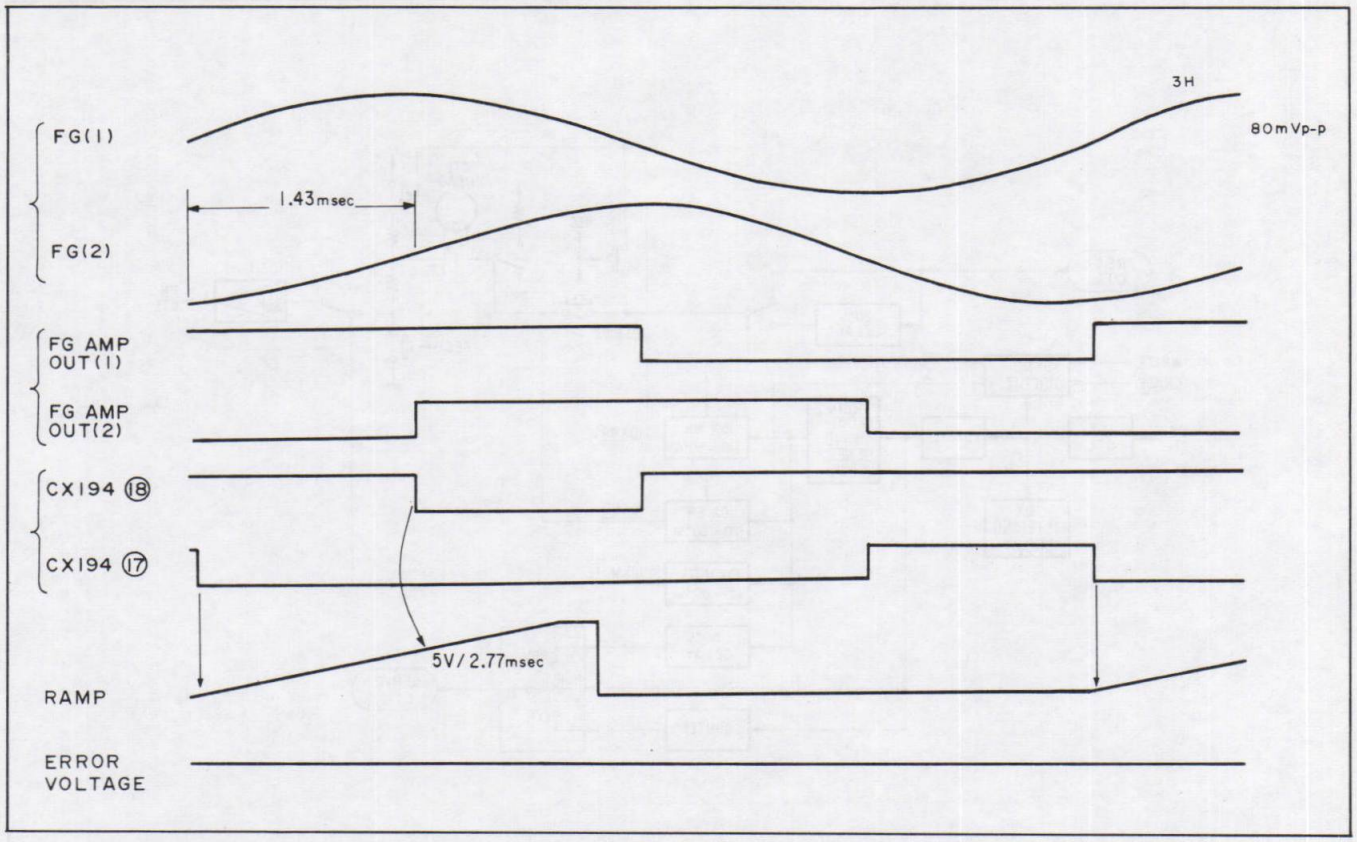


Fig. 3-14.

5) PG-A, PG-B and PG-S Timing Chart

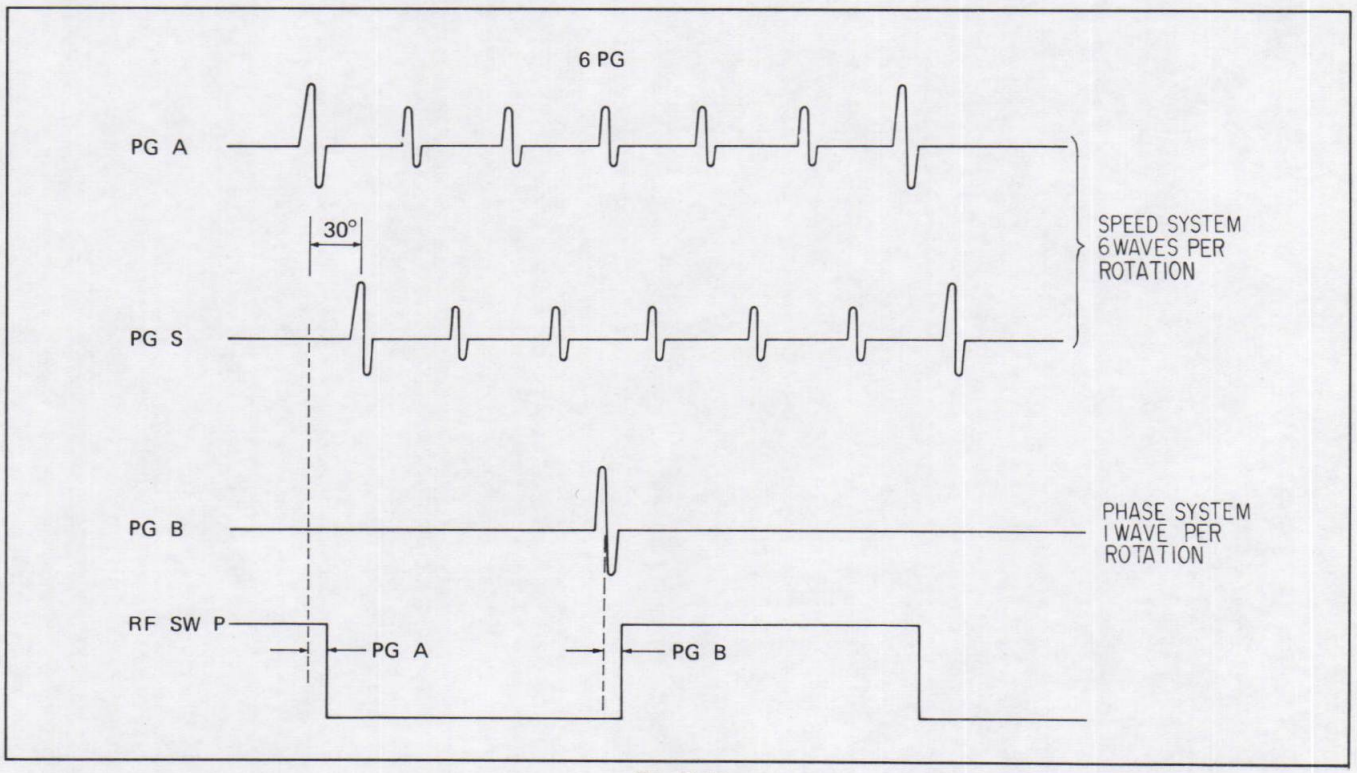


Fig. 3-15.

3-1-7. CTL INDEX Circuit

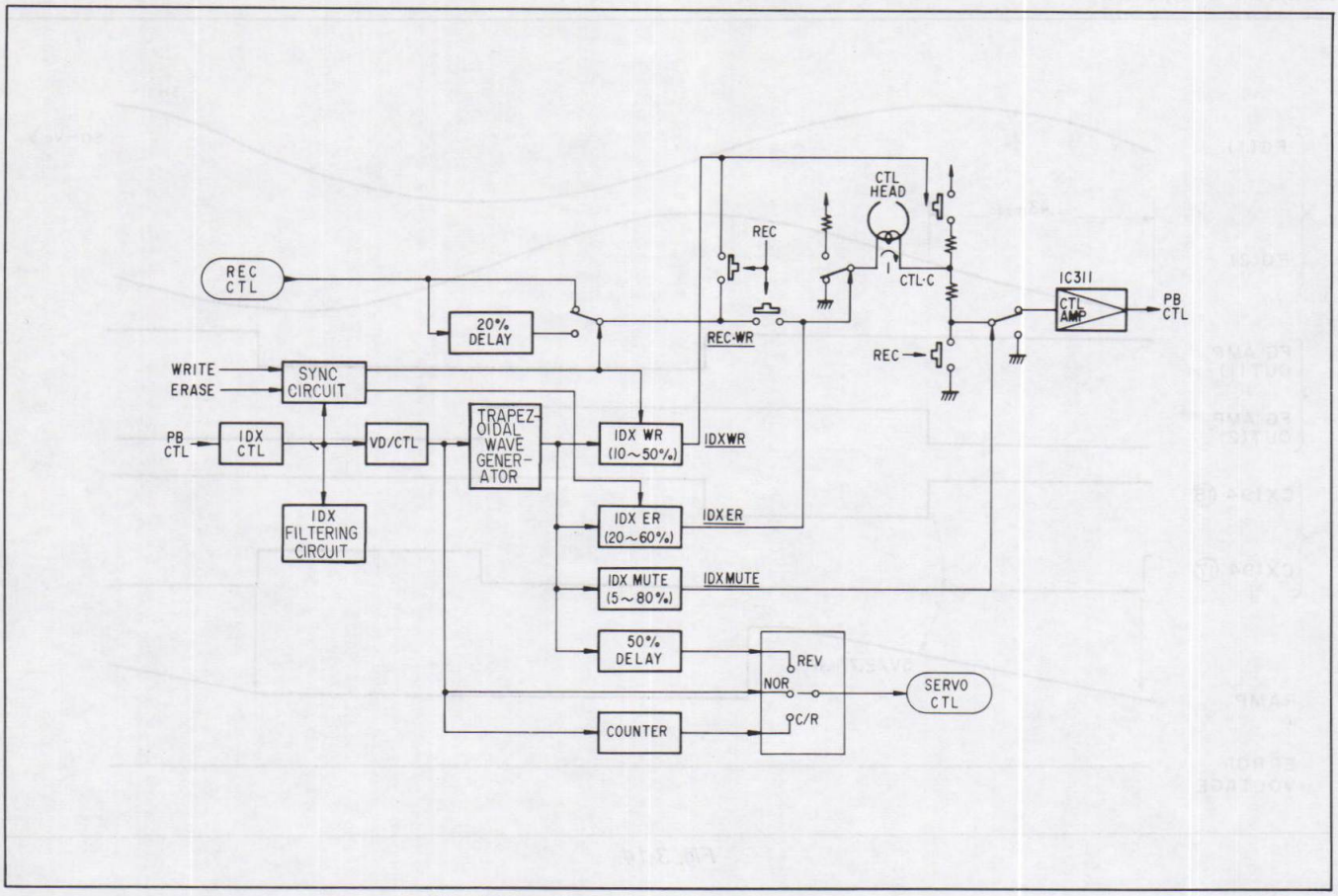


Fig. 3-16. CTL INDEX Circuit Block Diagram

The production of noise in the output is prevented by changing the threshold with respect to ⊕ feedback input noise. The servo, counter, etc. operate wrongly if noise is detected in the 25Hz CTL signal.

9V
RV317
RVS TRACON
IC309 BX1039
5V
0.022
33k
150k
270k
40.5k
47k
62k
150k
22k
Q5
Q6
Q4
Q3
560
2200
6800
68k
39k
C403 0.0033
C341 0.033
REC·PAUSE
INDEX WRITE
INDEX ERASE
IC310 BX3981
10k
68k
390k (±1.5%)
0.0047
Q8
Q9
100k
46.1k
30k
18.3k
22k
D2
D1
45k
150k
Q2
Q1
Q6
Q3
D3
D4
D5
30k
48.6k
5600
0.022 (15V)
68k
1M
Q5
Q4
C335 0.082
IC301 CX194A
CTL IN (L3)
REC CTL (L8)
15k
CTL HEAD
Q7
Q11
1000
1500
1000
CTL
IC308
100k
330k
2.2/50V
INDEX MUTE
IC311
PB CTL
5V REF
1.5k
1M
3.3M
75k
15k
22k
180k
IC307 (1/4)
IC307 (1/4)
CAP FWD
VD/CTL
INDEX CTL
REC·P
CUE + REV
INDEX WRITE
INDEX ERASE
IC312
COUNT DOWN
R9(1) R9(2) Ro(1) Ro(2)
AIN
BIN
QA QB QC QD
D311
CAP FWD
CUE+REV
Q10
Q11
Q12
47k

Fig. 3-17. CTL INDEX Circuit

1) REC CTL

During recording, the REC CTL signal produced by the V SYNC signal in IC301 is output from Pin 13 and is input to Pin 8 of IC309. While the REC CTL signal remains "L", Q6 is OFF, Q4, ON, and Q7, ON, and Q311 outside the IC, OFF, turning the voltage at Pin 11 to "H".
As Q6 is turned OFF, both Q3 and Q2 are turned OFF, and the voltage at Pin 3 goes "L", causing the CTL HEAD current to flow from the Pin 11 side to Pin 3 side (negative direction). Conversely, when the REC CTL signal is "H", Q7 turns OFF, and Q311 outside the IC turns ON, while the voltage at Pin 11 goes "L". When Q2 turns ON, the voltage on Pin 3 goes "H", causing the CTL HEAD current to flow from the Pin 3 side to the Pin 11 side (positive direction). As a result, a CTL signal with a 50% duty ratio is recorded. (See Fig. 3-18)
The weak signal produced at Pin 4 of IC309 is input to Pin 2 of IC311 and is output from Pin 6 after being amplified and shaped. The signal has its phase inverted twice by the REC·PAUSE signal on Pin 1 of IC307 and by the CAP FWD signal on Pin 5 and is output from Pin 4 as a VD/CTL signal to the system control circuit for use by the tape counter, etc.

2) PB CTL (Fig. 3-18)

During playback, the CTL HEAD output is input to Pin 3 of IC309 and is output from Pin 4. The output is input to Pin 2 of IC311 through IC308. The output is amplified by IC311 and is branched from Pin 1 to the slow servo circuit as the PB CTL signal. The signal is shaped into a square wave and is output from Pin 6. The output is branched to the system control circuit as an INDEX CTL signal after passing through Pins 2 and 3 of IC307. The system control circuit detects the INDEX signal (part of the CTL signal with a 20% duty) and performs APS (AUTO PROGRAM SEARCH). The output of Pin 3 of IC307 has its phase inverted by the CAP FWD signal ion Pin 5 to match the phases during the NORMAL and REVERSE playback modes and is output from Pin 4. The signal is branched to the system control circuit as a VD/CTL signal for use by the tape counter, etc. as in the recording mode. The VD/CTL signal is input to Pin 16 of IC301 through IC309 and will be utilized by the capstan phase servo.

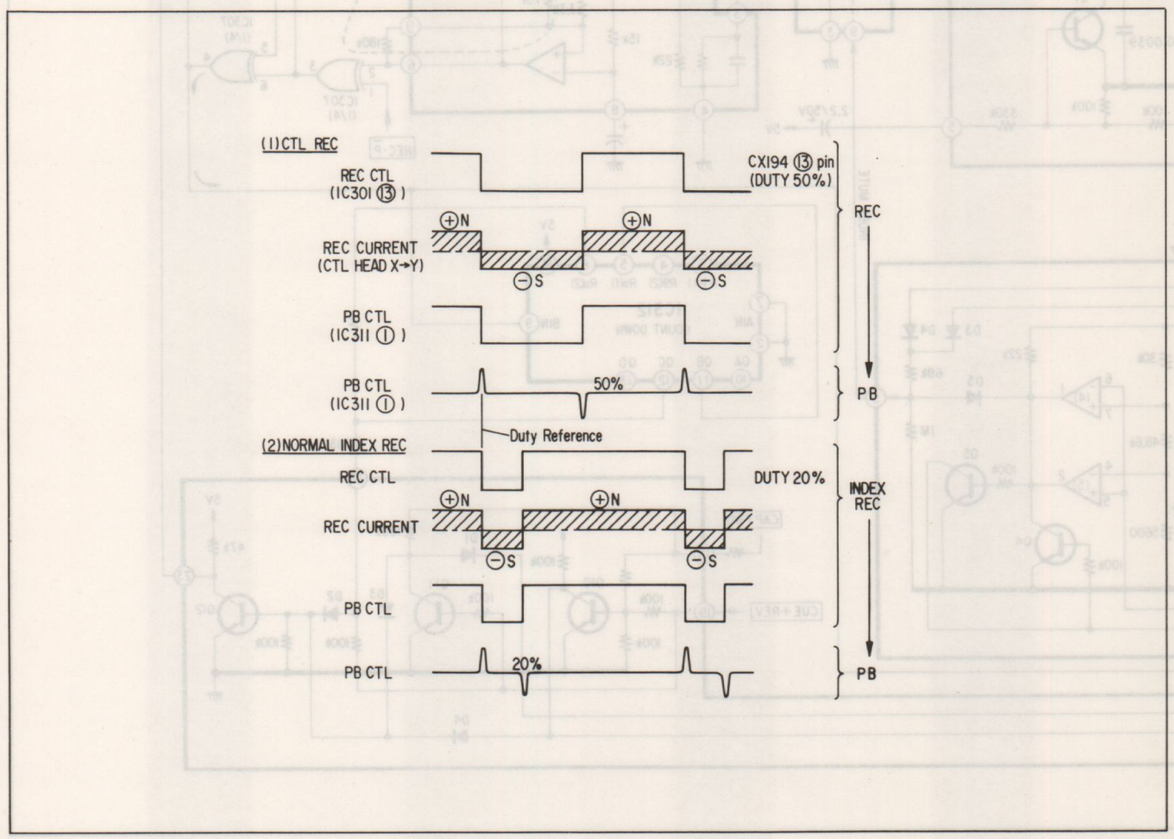


Fig. 3-18.

3) REC INDEX

The INDEX WRITE signal remains "H" for 9 seconds after starting recording to record the INDEX CTL signals. The REC CTL signals input to Pin 8 of IC309 are integrated by C341 and C403 that are connected to Pin 15 and are input to the negative side of the comparator 1. The signals are compared with the threshold level on the positive side of the comparator. The comparator output becomes a square wave with a constant phase difference with the REC CTL signal. The comparator is of open-collector and the comparator output is input to Q5 base only when the INDEX WRITE signal on Pin 7 is "H".
As a result, an INDEX CTL signal with a 20% duty ratio combining this signal and the REC CTL signal is obtained at the collectors of Q5 and Q6. This signal is recorded on the tape in the same manner as for the REC CTL signal. (See Figure 3-19)

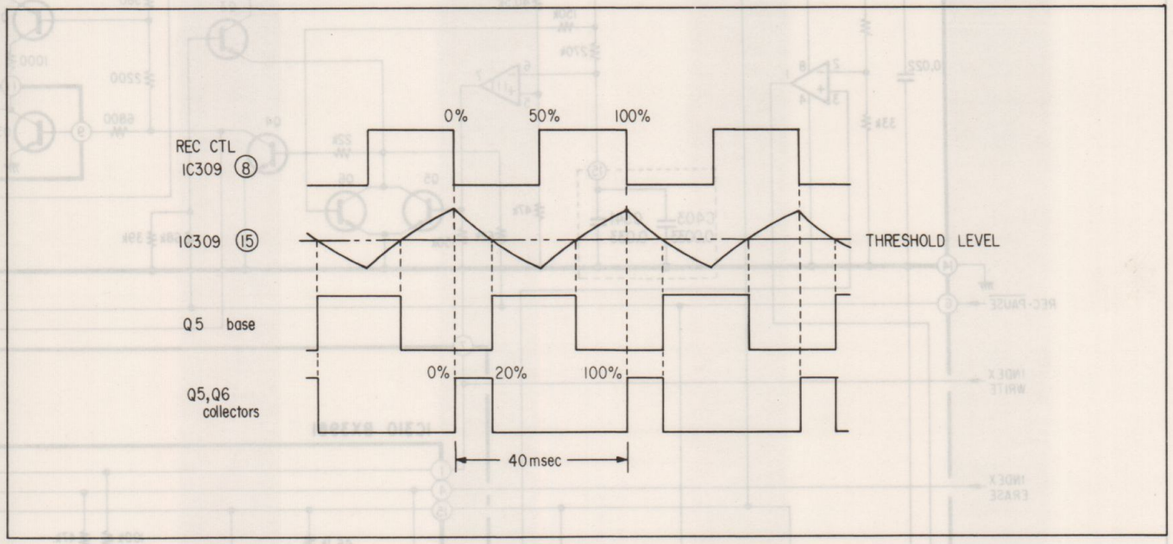


Fig. 3-19.

4) WRITING THE INDEX SIGNAL (DURING PLAYBACK) (Figs 3-20 and 3-21)

The INDEX WRITE signal remains "H" for 9 seconds and the INDEX signal is written on the tape when the APS MARK (INDEX WRITE) button is pressed in the desired position during playback. The VD/CTL signal produced from the playback PB CTL signal (Pin 4 of IC307) is input to Pin 17 of IC309. The phase of the signal is inverted by Q9 of IC309 and is differenctiated to switch Q8 on and off. C335 is connected to the Q8 collector (Pin 13 of IC309), and a saw tooth wave is produced. (See Fig. 3-18) The saw tooth wave is input to Comparators 2 and 3 inside IC310 through Pin 16 of IC310. A pulse whose level changes to "H" in a position 20 to 60% up the saw tooth rise is obtained through the threshold levels of these comparators. These comparators are open-collector type, and external power has to be supplied to the output terminals. The INDEX WRITE signal from Pin 1 of IC310 is used as the power for this purpose.
The comparator output switches on Q2 in IC309 through Q1, Pin 2 of IC310, and Pin 2 of IC309. For this reason, a current in the normal direction flows in the CTL head and changes the duty ratio of the CTL signals recorded on the tape from 50 to 20%.
The diode, resistor, and capacitor between Pin 2 of IC310 and Pin 2 of IC309 makes the rise of the pulse at its 60% position gentle and prevents whiskers from being produced at the 60% position gentle and prevents whiskers from being produced at the 60% position of the INDEX CTL signals recorded on the tape.

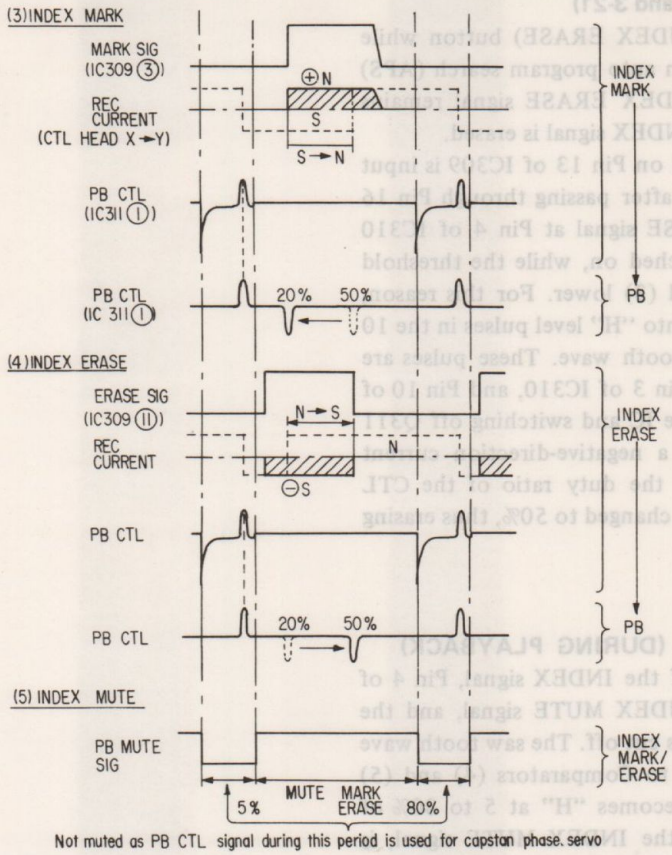


Fig. 3-20.

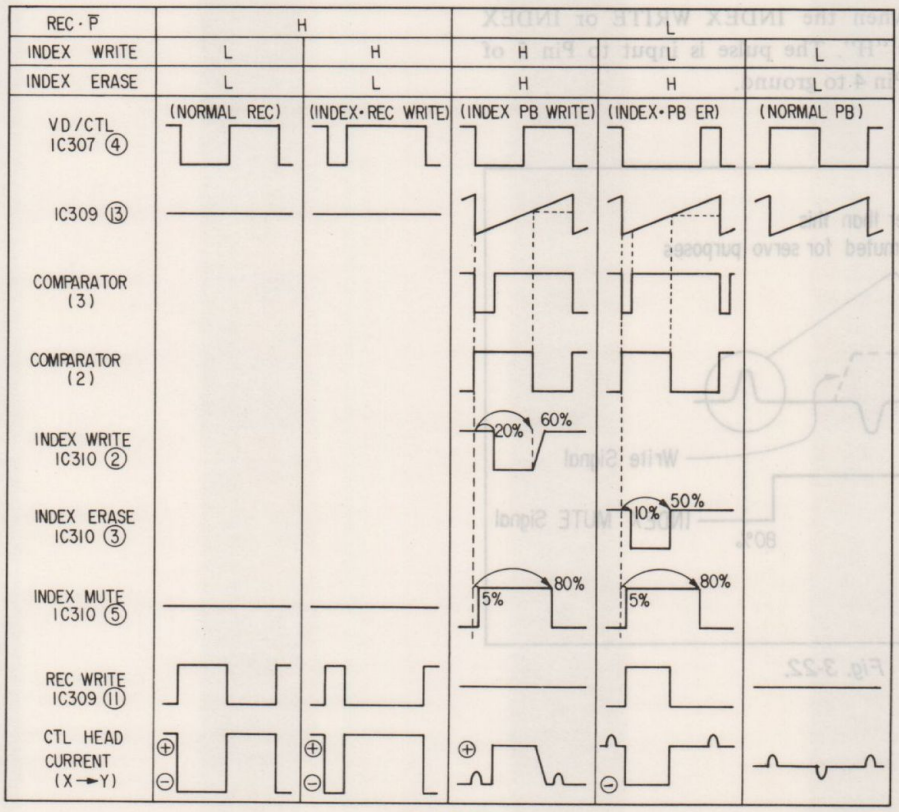


Fig. 3-21.

5) ERASING INDEX SIGNALS (DURING PLAYBACK) (Figs. 3-20 and 3-21)

Pressing the APS ERASE (INDEX ERASE) button while the APS display is lit after an auto program search (APS) operation is finished, the INDEX ERASE signal remains "H" for 15 seconds, and the INDEX signal is erased.

The saw tooth wave produced on Pin 13 of IC309 is input to the Comparators 2 and 3 after passing through Pin 16 of IC310. The INDEX ERASE signal at Pin 4 of IC310 remains "H", and Q6 is switched on, while the threshold levels of Comparators (2) and (3) lower. For this reason, the comparator outputs turn into "H" level pulses in the 10 to 50% position of the saw tooth wave. These pulses are input in IC309 through Q2, Pin 3 of IC310, and Pin 10 of IC309, switching on Q7 in the IC and switching off Q311 outside the IC. As a result, a negative-direction current flows in the CTL head, and the duty ratio of the CTL signal recorded on the tape is changed to 50%, thus erasing the INDEX signal.

6) INDEX MUTE SIGNAL (DURING PLAYBACK)

During writing and erasing of the INDEX signal, Pin 4 of IC308 is grounded by the INDEX MUTE signal, and the input of PB CTL AMP IC311 is cut off. The saw tooth wave on Pin 13 of IC309 is input to Comparators (4) and (5) in IC310, and a pulse that becomes "H" at 5 to 80% of the saw tooth rise, that is, the INDEX MUTE signal, is produced by the threshold level of the saw tooth wave. (See Fig. 3-22). The pulse is switched by D5 and is output from Pin 5 only when the INDEX WRITE or INDEX ERASE signal stays "H". The pulse is input to Pin 5 of IC308 and switches Pin 4 to ground.

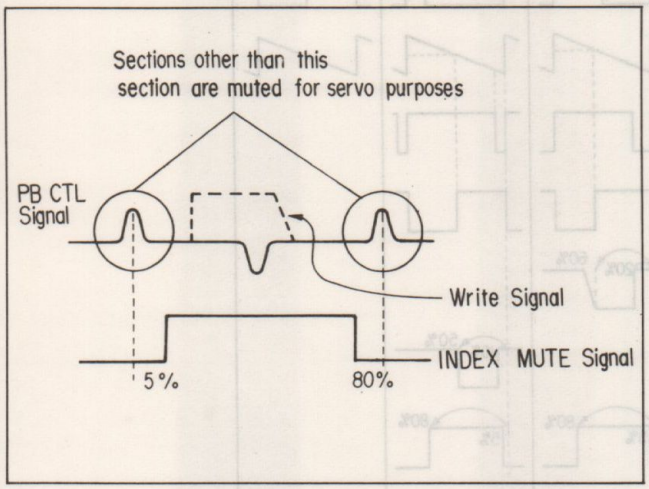


Fig. 3-22.

3-2. REEL SERVO CIRCUIT

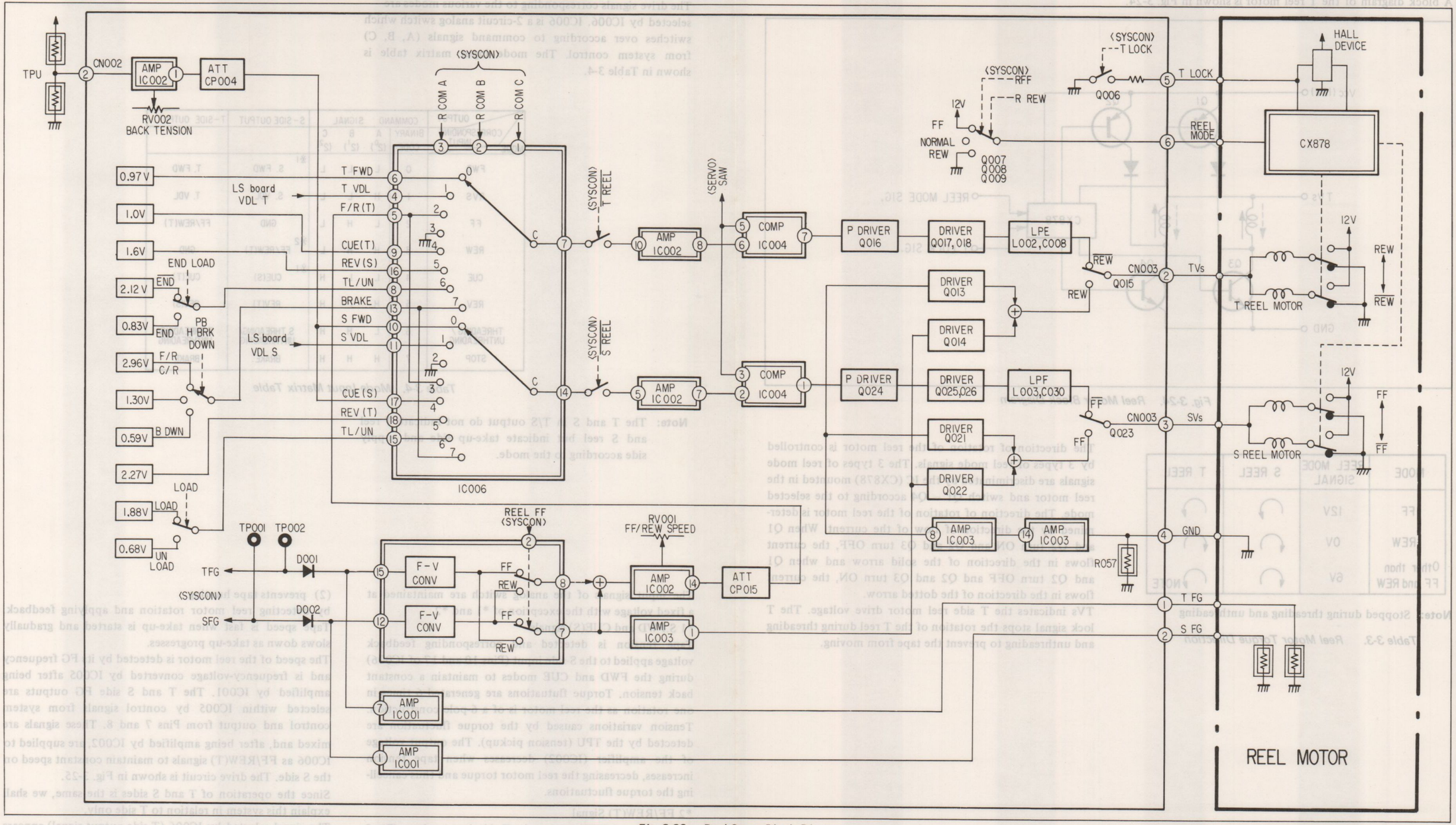


Fig. 3-23. Reel-Servo Block Diagram

The reel-servo circuit is contained in the SS-11 Board. In the SL-C9E, both the supply side (S) and take-up side (T) reels are driven directly by the reel motors. Fig. 3-23 shows a block diagram of the reel-servo circuit.

3-2-1. Reel Motor

A block diagram of the T reel motor is shown in Fig. 3-24.

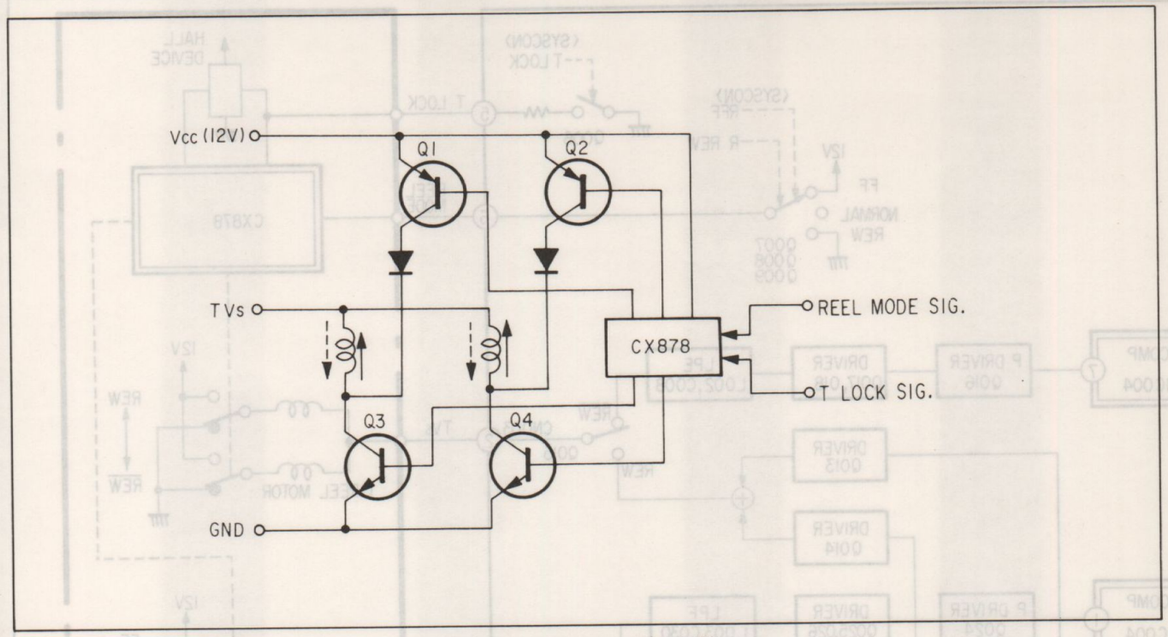


Fig. 3-24. Reel Motor Block Diagram

MODE	REEL MODE SIGNAL	S REEL	T REEL
FF	12V	↷	↷
REW	0V	↶	↶
Other than FF and REW	6V	↶	↶ NOTE

Note: Stopped during threading and unthreading

Table 3-3. Reel Motor Torque Direction

The direction of rotation of the reel motor is controlled by 3 types of reel mode signals. The 3 types of reel mode signals are discriminated by the IC (CX878) mounted in the reel motor and switch Q1 – Q4 according to the selected mode. The direction of rotation of the reel motor is determined by the direction of flow of the current. When Q1 and Q2 turn ON and Q2 and Q3 turn OFF, the current flows in the direction of the solid arrow and when Q1 and Q2 turn OFF and Q2 and Q3 turn ON, the current flows in the direction of the dotted arrow.

TVs indicates the T side reel motor drive voltage. The T lock signal stops the rotation of the T reel during threading and unthreading to prevent the tape from moving.

3-2-2. Drive Circuit

The drive signals corresponding to the various modes are selected by IC006. IC006 is a 2-circuit analog switch which switches over according to command signals (A, B, C) from system control. The mode input matrix table is shown in Table 3-4.

OUTPUT / CORRESPONDING INPUT / MODE	COMMAND SIGNAL BINARY CODE	A (2^0)	B (2^1)	C (2^2)	S-SIDE OUTPUT	T-SIDE OUTPUT
FWD	0	L	L	L	※1 S. FWD	T. FWD
RVS	1	H	L	L	S. VDL	T. VDL
FF	2	L	H	L	GND	FF/REW(T)
REW	3	H	H	L	※2 FF/REW(T)	GND
CUE	4	L	L	H	※1 CUE(S)	CUE(T)
REV	5	H	L	H	REV(T)	REV(S)
THREADING / UNTHREADING	6	L	H	H	S. THREADING/ UNTHREADING	T. THREADING/ UNTHREADING
STOP	7	H	H	H	BRAKE	BRAKE

Table 3-4. Mode Input Matrix Table

Note: The T and S in T/S output do not indicate T reel and S reel but indicate take-up side and supply side according to the mode.

The input signals of the analog switch are maintained at a fixed voltage with the exception of *1 and *2.

*1 S.FWD and CUE(S) signals

Tape tension is detected and corresponding feedback voltage applied to the S-side input (Pins 10 and 17 of IC006) during the FWD and CUE modes to maintain a constant back tension. Torque flutuations are generated 6 times in one rotation as the reel motor is of a 6-pole construction. Tension variations caused by the torque fluctuation are detected by the TPU (tension pickup). The output voltage of the amplifier (IC002) decreases when tape tension increases, decreasing the reel motor torque and thus cancelling the torque fluctuations.

*2 FF/REW(T) Signal

In the FF and REW modes, the T-side input voltage (Pin 5 of IC006)

(1) makes rotation on the S-side constant and

(2) prevents tape hunting

by detecting reel motor rotation and applying feedback. Tape speed is fast when take-up is started and gradually slows down as take-up progresses.

The speed of the reel motor is detected by its FG frequency and is frequency-voltage converted by IC005 after being amplified by IC001. The T and S side FG outputs are selected within IC005 by control signals from system control and output from Pins 7 and 8. These signals are mixed and, after being amplified by IC002, are supplied to IC006 as FF/REW(T) signals to maintain constant speed on the S side. The drive circuit is shown in Fig. 3-25.

Since the operation of T and S sides is the same, we shall explain this system in relation to T side only.

The signal selected by IC006 (T-side output signal) appears as an output at Pin 7. Q010 starts and stops the T reel by means of ON/OFF control signals according to signals from

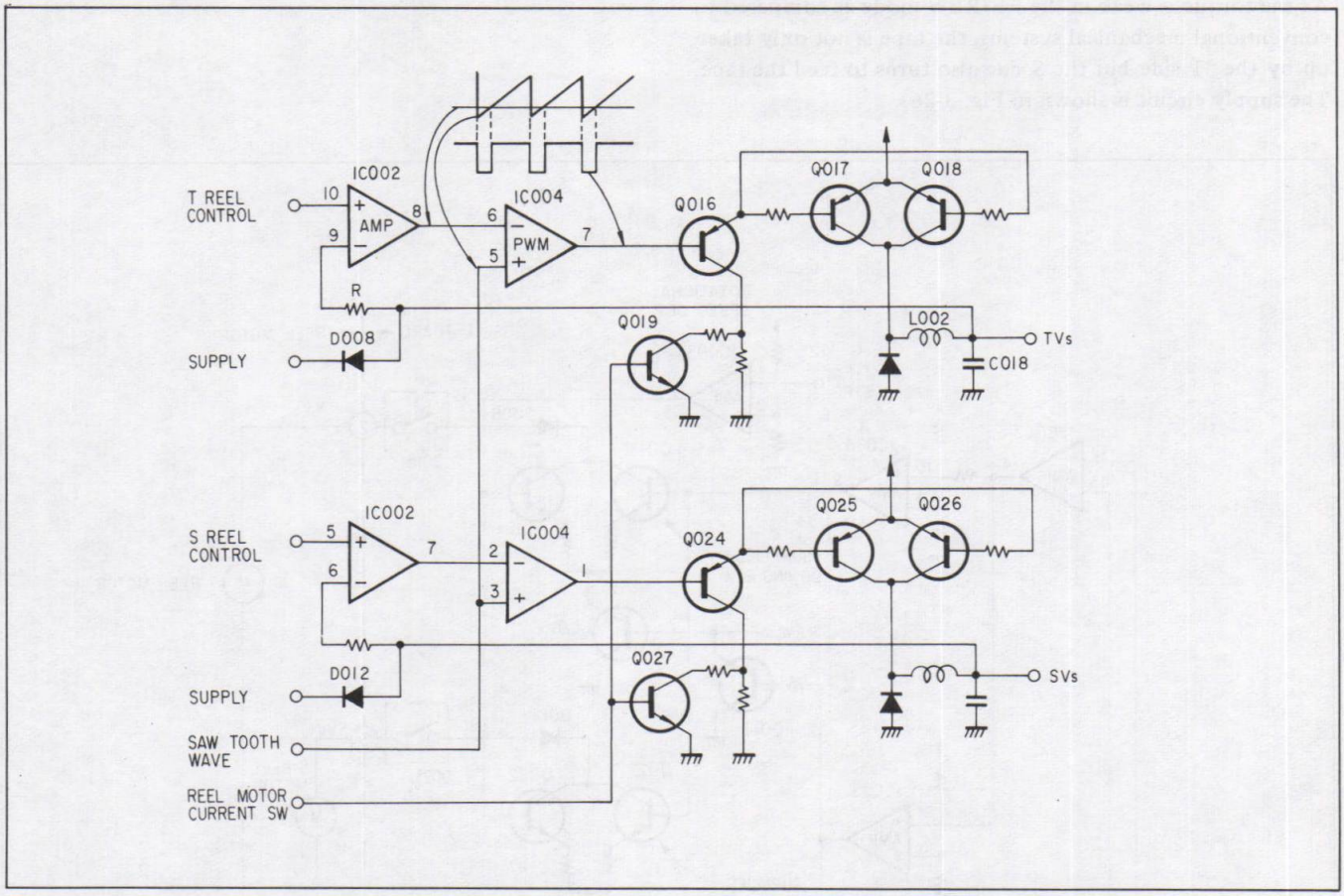


Fig. 3-25. Reel Motor Drive Circuit

system control. When "H" signals are received, the $\overline{\text{T REEL}}$ is stopped and when "L" signals are received, the reel is rotated. The output signal from Pin 7 is supplied to Pin 6 of comparator IC004 after amplification by IC002. On one hand, the saw tooth wave supplied to Pin 5 is converted to PWM signals which appear as outputs at Pin 7. Q016–Q018 are driven by this output signal and, after being converted to DC by the LPF composed of L002 and C018, the voltage derived (TVs) is used to drive the T reel.

Also, when the T reel output signal (output signal on Pin 7) in the drive circuit increases, TVs also increase and the ratio is set to twice the input by R shown in Fig. 3-25. Also, during FF, REW and REV modes, a larger drive torque (current) will be required on the T side compared with other modes. In these modes, the current flow in the T side is detected and the drive circuit current increased by turning Q019 or Q027 ON.

3-2-3. Supply Circuit

As the torque is weak in the FF/REW mode as compared to conventional mechanical systems, the tape is not only taken up by the T side but the S side also turns to feed the tape. The supply circuit is shown in Fig. 3-26.

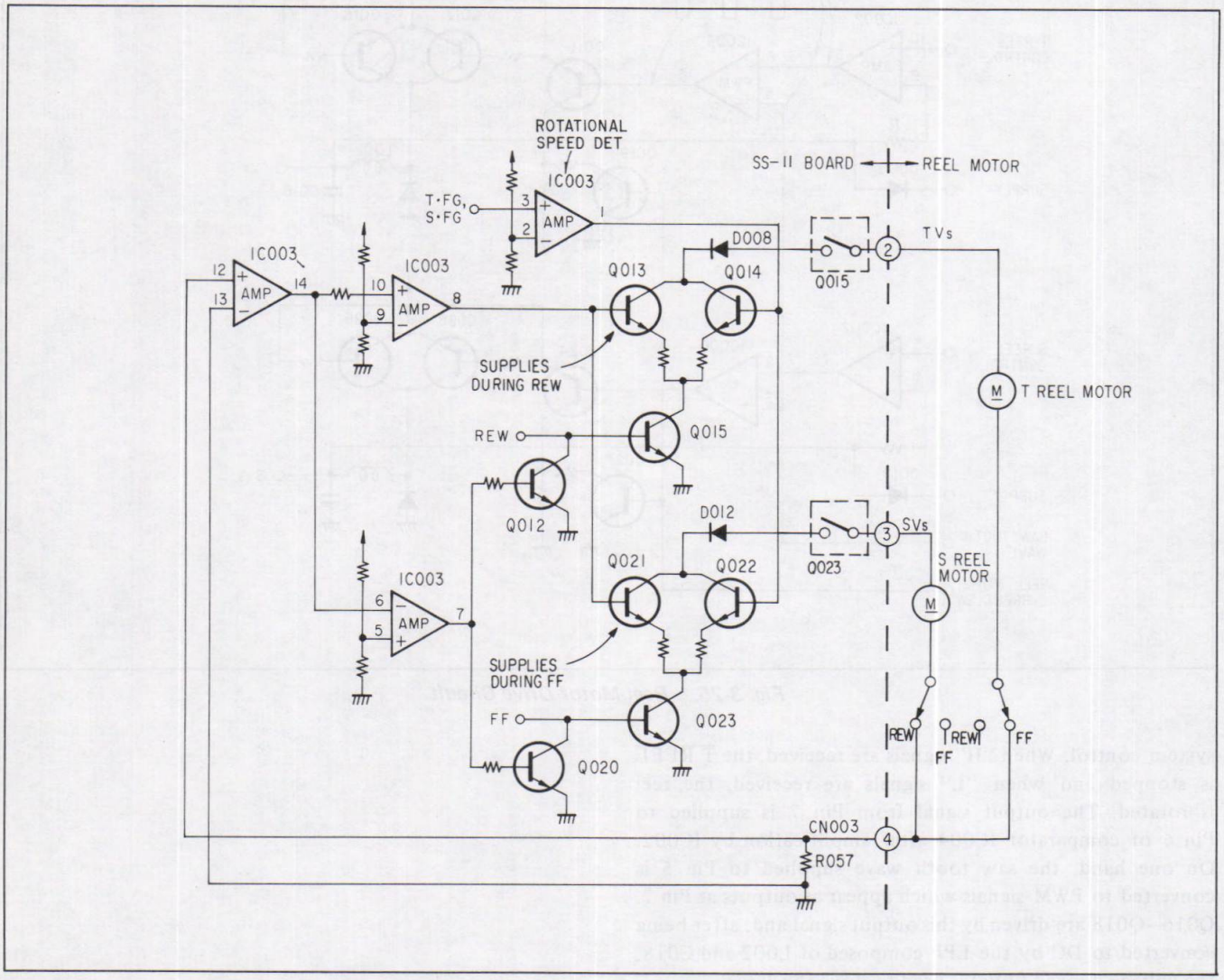


Fig. 3-26. Supply Circuit

As both T and S sides operate in the same way an explanation only in relation to the T side will be made here. When set to REW mode, the drive circuit turns OFF, Q015 turns ON and the T reel motor is connected to Q013 and Q014 through D008. Q013 and Q014 now control the currnet flowing in the T reel motor. Q013 uses the reel motor current and Q014 uses the reel motor revolutions as their respective control signals.

1) Current Detection

The reel motor ground is connected to the ground line of the circit from pin 4 of CN003 through resistor R057 (0.1Ω). R057 is used for current detection purposes and the voltage developed across this resistor is amplified by IC003 and applied to the base of Q013 as control signals.

2) Revolution Detection

As in the case of the drive circuit, the number of revolutions is detected by the FG signal. If the FG frequency increases, the reel motor load increases and constant speed is thus maintained by controlling Q014.

3-3. VARIABLE SPEED PB CIRCUIT

The variable speed PB circuit is contained in the JR-1 Board. The block diagram is shown in Fig. 3-27 and the timing chart in Fig. 3-28.

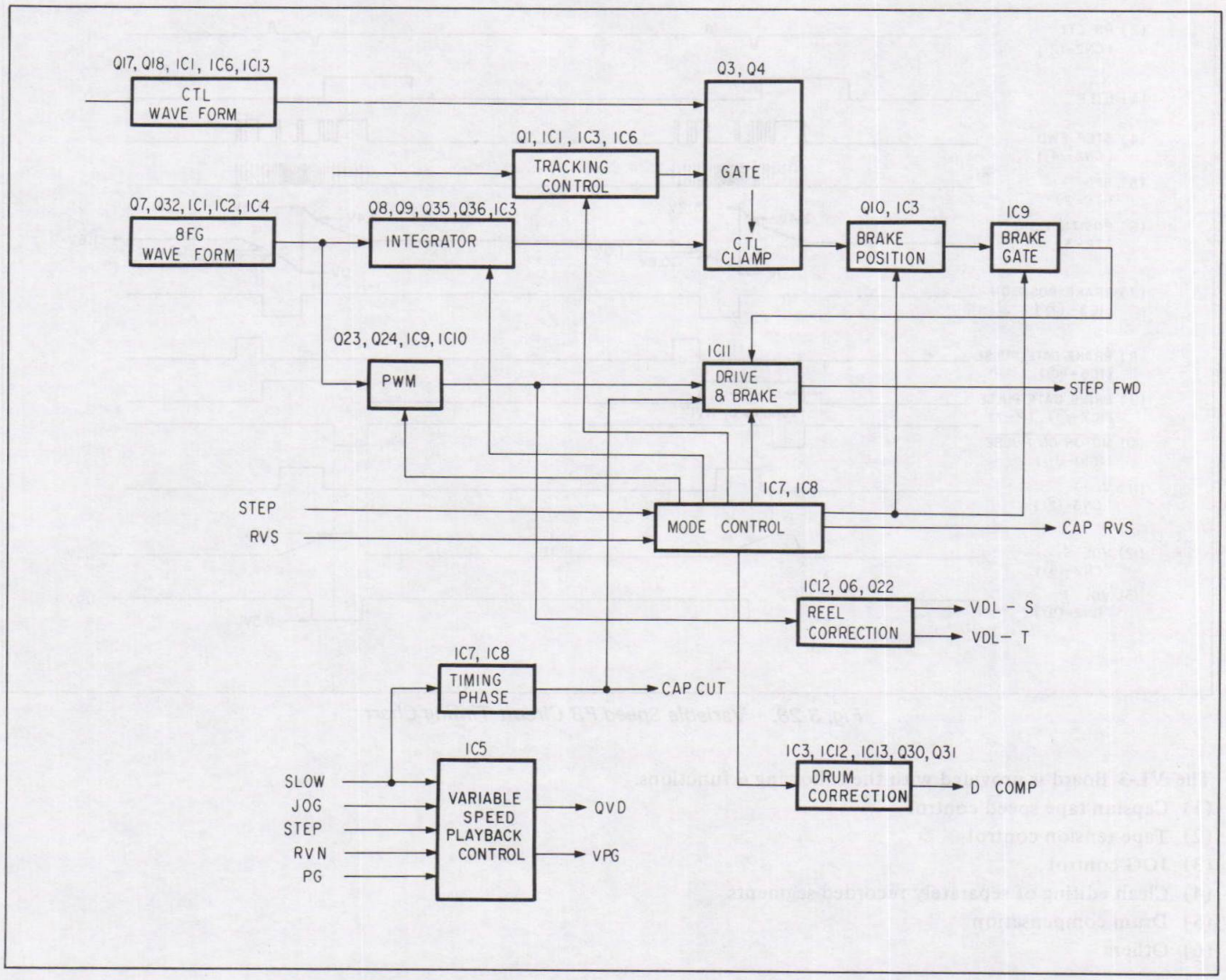


Fig. 3-27. Variable Speed PB Circuit Block Diagram

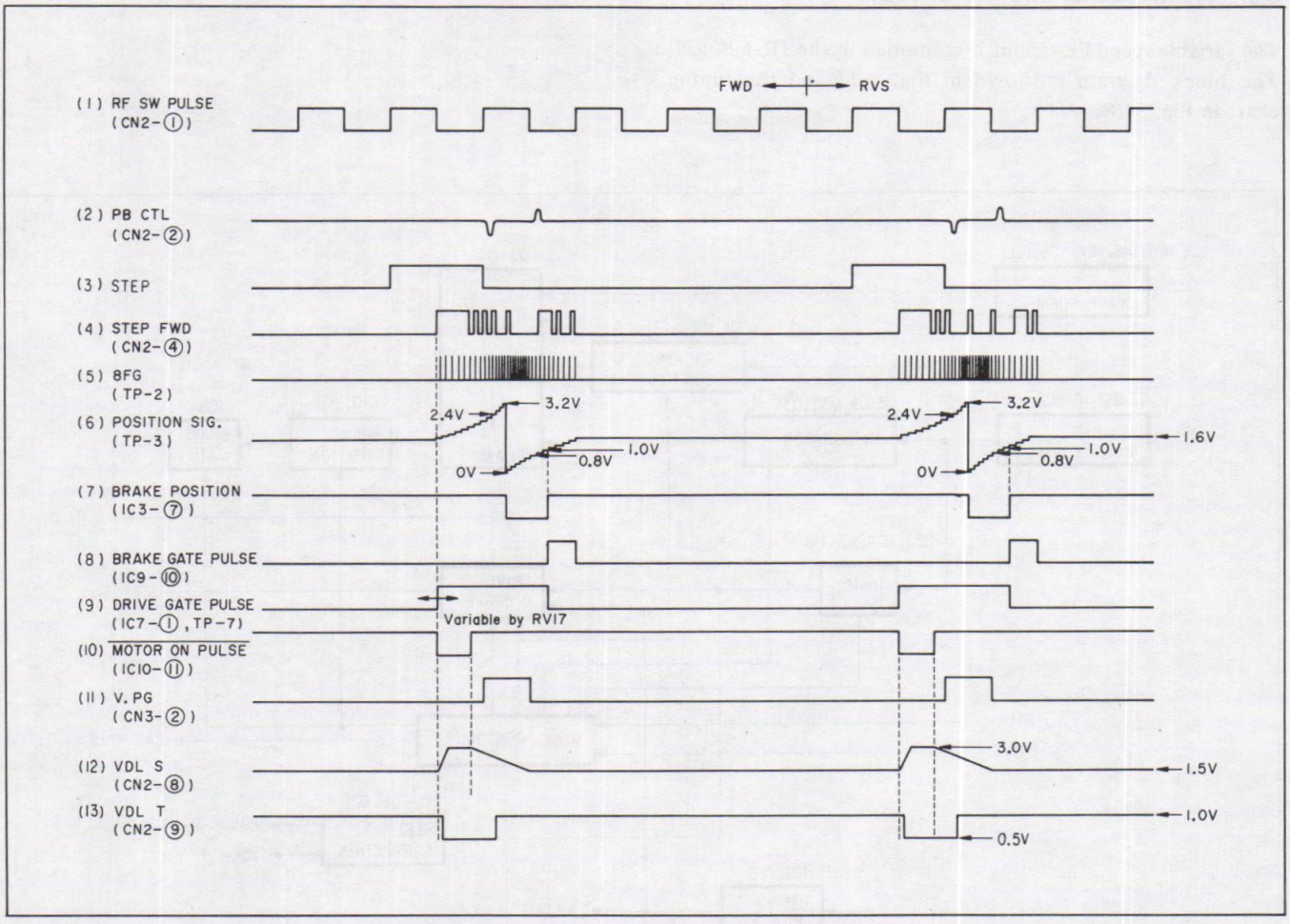


Fig. 3-28. Variable Speed PB Circuit Timing Chart

The VL-3 Board is provided with the following 6 functions.

(1) Capstan tape speed control
(2) Tape tension control
(3) JOG control
(4) Clean editing of separately recorded segments
(5) Drum compensation
(6) Others

3-3-1. Capstan Tape Speed Control

Fig. 3-29, shows a block diagram of this system.

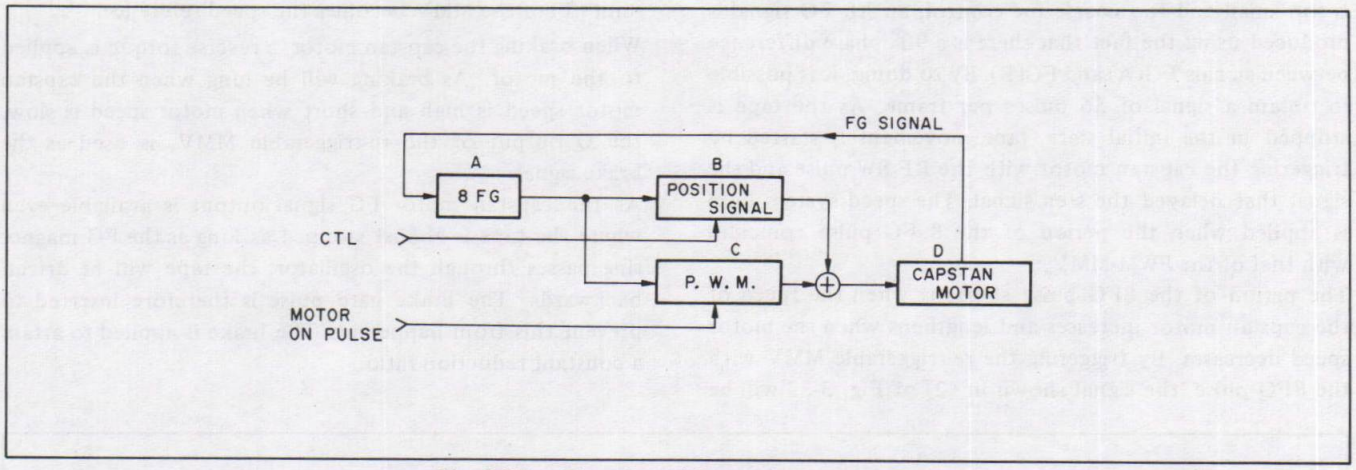


Fig. 3-29. Tape Speed Control Block Diagram

In Fig. 3-30, A→B→D corresponds to a phase system loop and A→C→D to a speed system loop. The CTL signal is used as the reference signal for the phase system and the time constant of the PWM multi is used as the reference signal for the speed system. The brake position (indicates a certain portion of the voltage of the position signal, see Fig. 3-39) is the speed system error plus the phase error.

1) Tape Movement During Step Feeding

Fig. 3-30, shows the tape movement during step feeding.

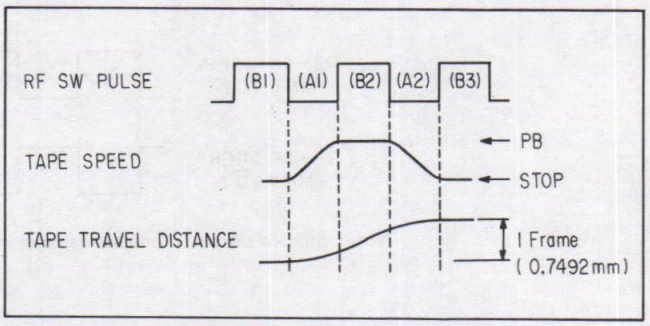


Fig. 3-30. Tape Movement

Tape movement commences at the point where the RF SW pulse begins to fall (B1) and attains normal playback speed at (B2). Brake is applied from the point where the RF SW pulse begins to fall at (B2) and the tape comes to a stop at the point where the pulse begins to rise at (A2). The braking method used is to apply torque in the opposite direction of the capstan motor. The DRIVE/BRAKE signals of the capstan motor are shown in Fig. 3-31.

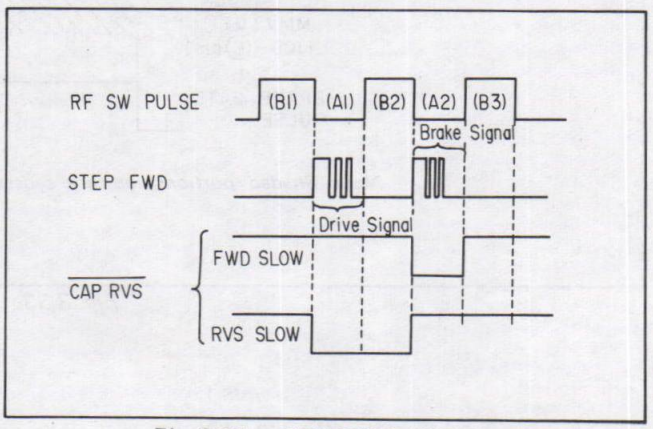


Fig. 3-31. DRIVE/BRAKE Signal

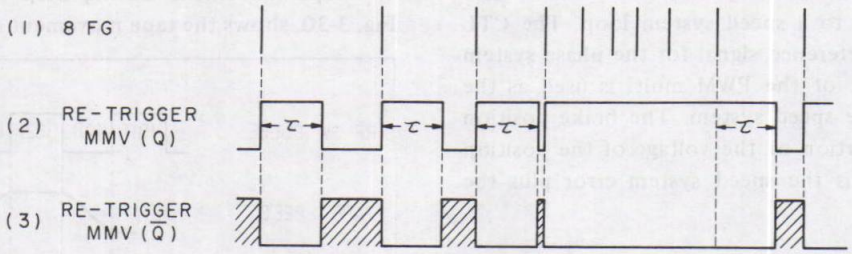
2) Speed System Loop

As the FG signal of the capstan motor is 175Hz, 7Hz (tape moves 0.7492mm) are obtained per frame. However, as 7Hz is too small and too coarse for control, an X8 FG signal is produced using the fact that there is a 90° phase difference between signals FG(A) and FG(B). By so doing, it is possible to obtain a signal of 56 pulses per frame. As the tape is stopped in the initial state, tape movement is started by triggering the capstan motor with the RF SW pulse and the signal that delayed the step signal. The speed system loop is applied when the period of the 8 FG pulse coincides with that of the PWM-MMV.

The period of the 8FG pulse shortens when the speed of the capstan motor increases and lengthens when the motor speed decreases. By triggering the re-triggerable MMV with the 8FG pulse, the signal shown in (2) of Fig. 3-32 will be obtained and constant speed is possible by driving the capstan motor with signal(3) as drive will be long when speed is slow and short when speed is fast. The time constant (T) of the MMV becomes the speed reference.

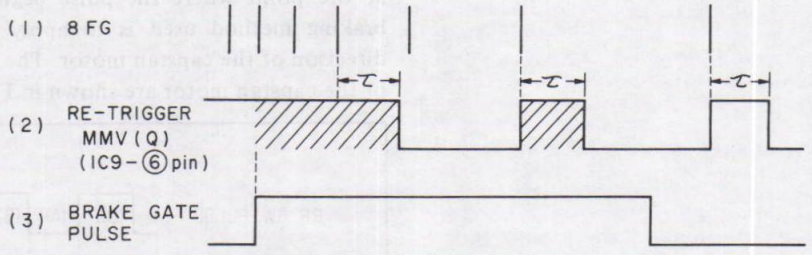
When braking the capstan motor, a reverse torque is applied to the motor. As braking will be long when the capstan motor speed is high and short when motor speed is slow, the Q output of the re-triggerable MMV, is used as the brake signal.

As the capstan motor FG signal output is available even where the tape is almost stopped as long as the FG magnet ring passes through the oscillator, the tape will be driven backwards. The brake gate pulse is therefore inserted to prevent this from happening. The brake is applied to attain a constant reduction ratio.



Note: *Shaded portions indicate capstan motor drive sections*

Fig. 3-32. Re-trigger MMV



Note: *Shaded portions indicate capstan motor braking sections.*

Fig. 3-33. Braking Method

i) 8 FG Pulse Generating Circuit

The 8 FG pulse is generated by utilizing the fact that there is a 90° phase difference between FG(A) and FG(B). As the input of the OP Amp is a differential input, the respective FG signal waveform is shaped at about 45°. The timing charts are shown in Fig. 3-34 and 3-35.

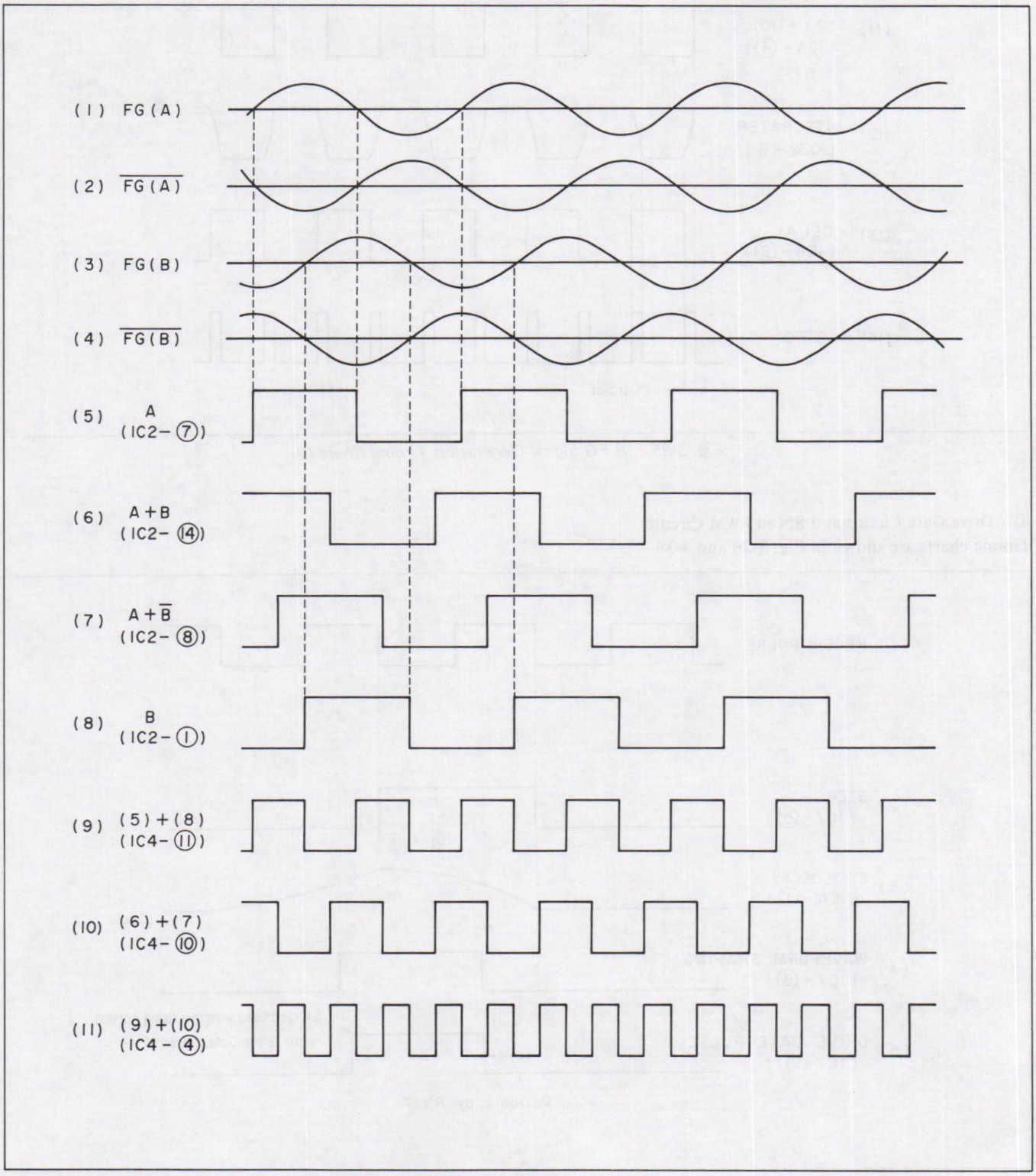


Fig. 3-34. 8 FG Signal Generation Timing Chart (1)

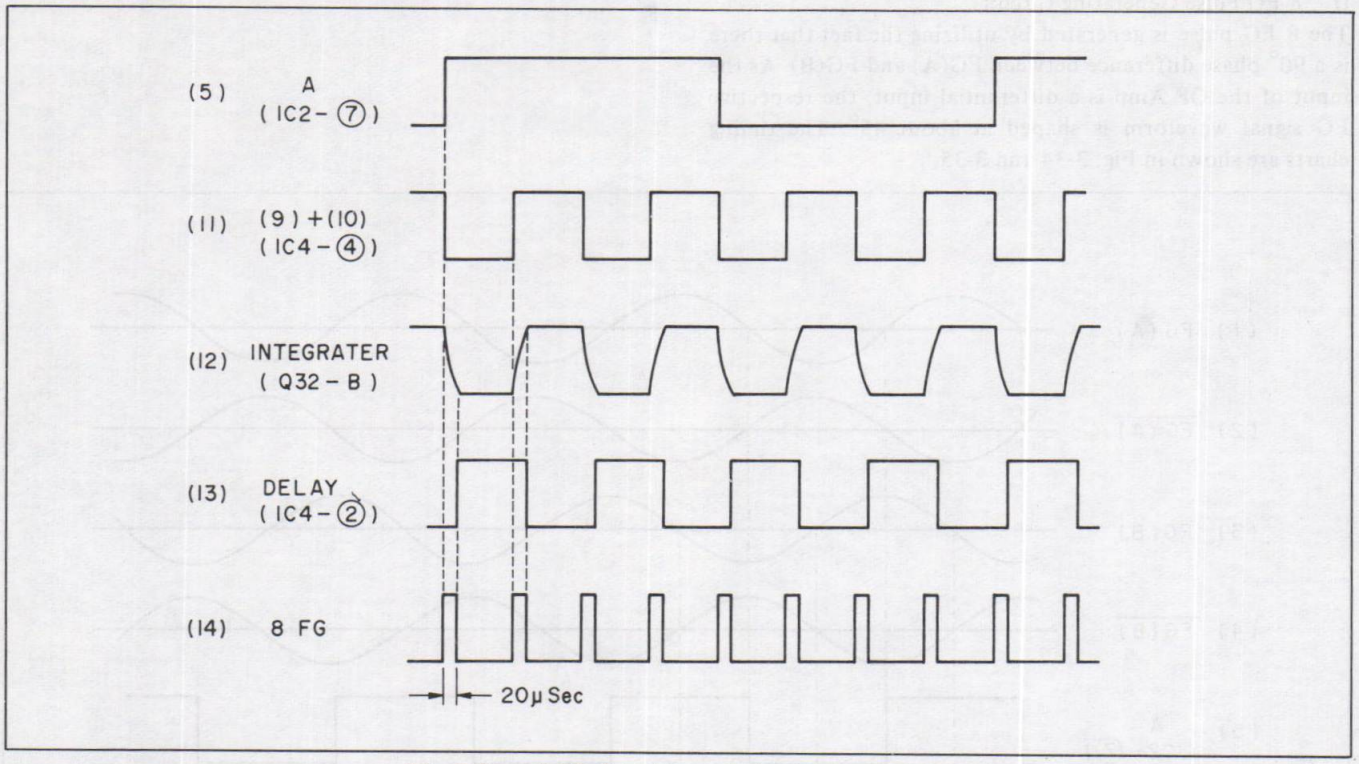


Fig. 3-35. 8 FG Signal Generation Timing Chart (2)

ii) Drive Gate Circuit and Speed PWM Circuit
Timing charts are shown in Fig. 3-36 and 3-38.

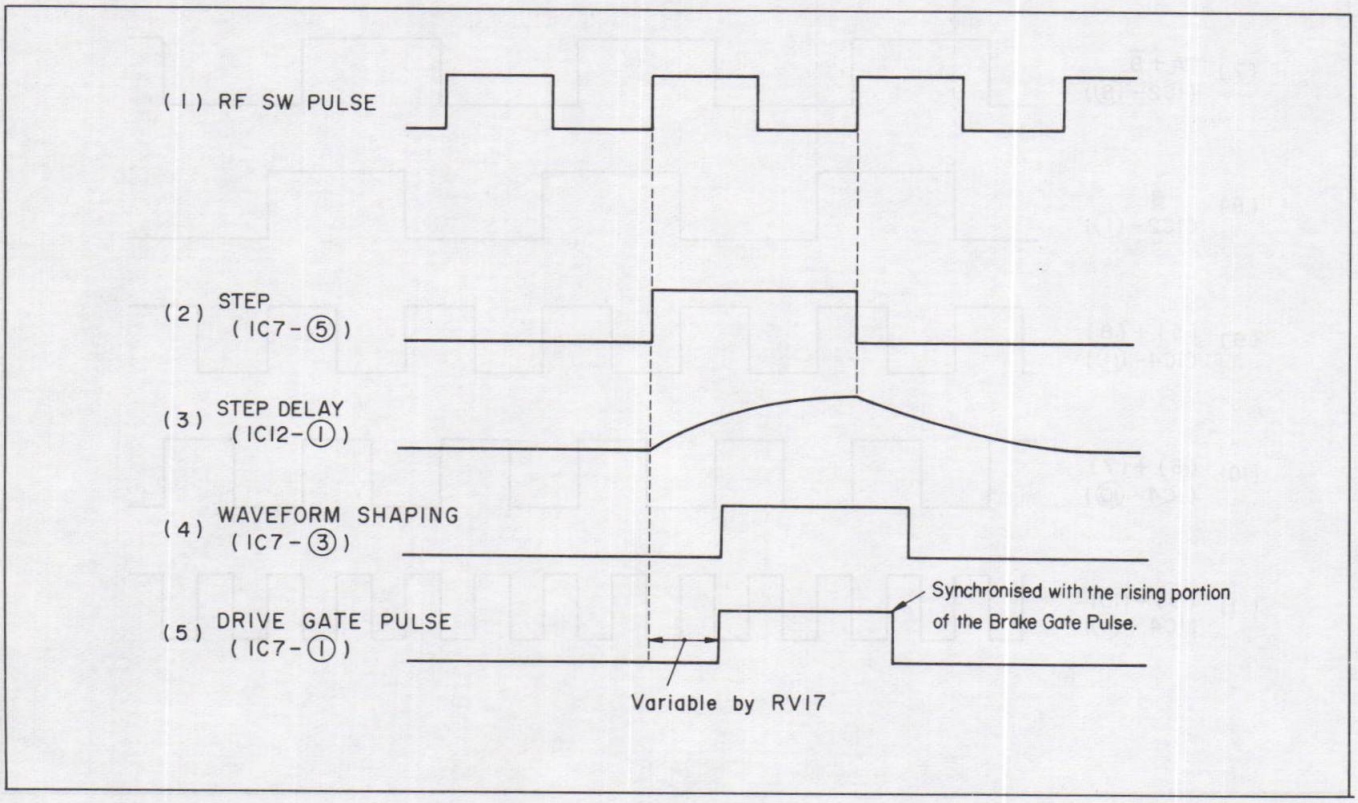


Fig. 3-36.

The DRIVE GATE PULSE is produced in the D-type flip-flop circuit (IC7) by the step pulse and step delay pulse and appears as an output at Pin 2 of IC7. This D-FF is reset by the brake gate pulse from Pin 4. (In the servo mode variable speed playback operation, a SLOW signal is applied to Pin 12 of IC7 to inhibit outputs of the DRIVE GATE PULSE.)

The FF (Pin 8 of IC10 . . . . . set, Pin 13 . . . . . reset) is triggered by the DRIVE GATE PULSE and drops the MOTOR ON PULSE. The MOTOR ON PULSE rises with the appearance of a matching pulse on Pin 3 of IC10. The width of the MOTOR ON PULSE is selected to obtain a time of about 70% (C25/C25 + C26) of the final speed. The time constants are changed by turning Q24 On/OFF with the MOTOR ON PULSE. (See Fig. 3-37)

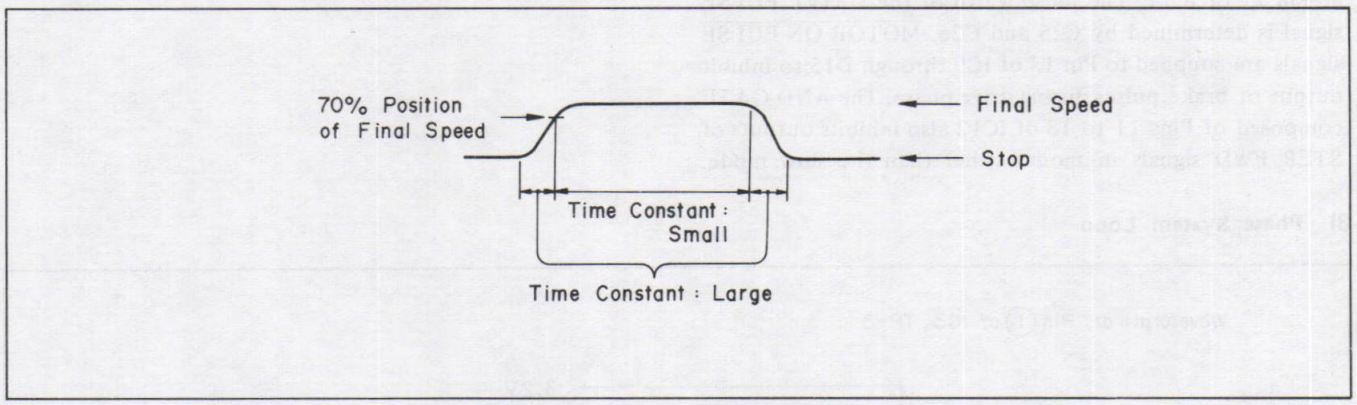


Fig. 3-37. Time Constant and Tape Speed

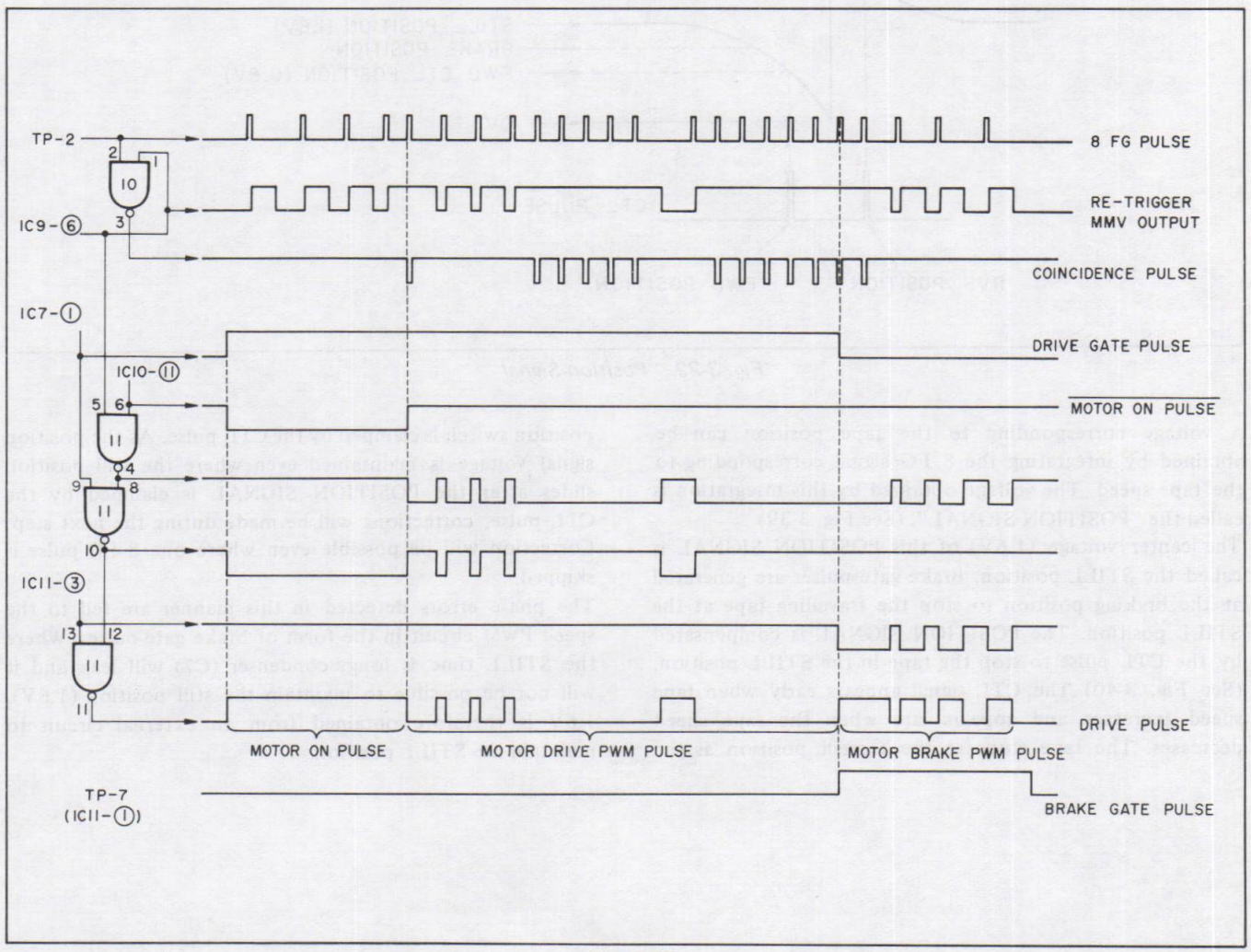


Fig. 3-38.

The $\overline{\text{MOTOR ON PULSE}}$ appears as an output at TP8 in the form of a STEP FWD signal after passing through IC11 and IC12. When the $\overline{\text{MOTOR ON PULSE}}$ is reset by the output of the matching pulse, the output of PWM-MMV (Pin 13 of IC9) passes through IC11 and IC12 and appears at TP8.

When the output of the brake gate pulse appears at Pin 10 of IC9, TP7, outputs of the DRIVE PULSE signal appear at Pin 11 of IC11. The pulse width of the DRIVE PULSE signal is determined by C25 and C26. $\overline{\text{MOTOR ON PULSE}}$ signals are supplied to Pin 13 of IC9 through D15 to inhibit output of brake pulses during drive phase. The AND GATE composed of Pins 11 to 13 of IC12 also inhibits outputs of STEP FWD signals in modes other than the slow mode.

3) Phase System Loop

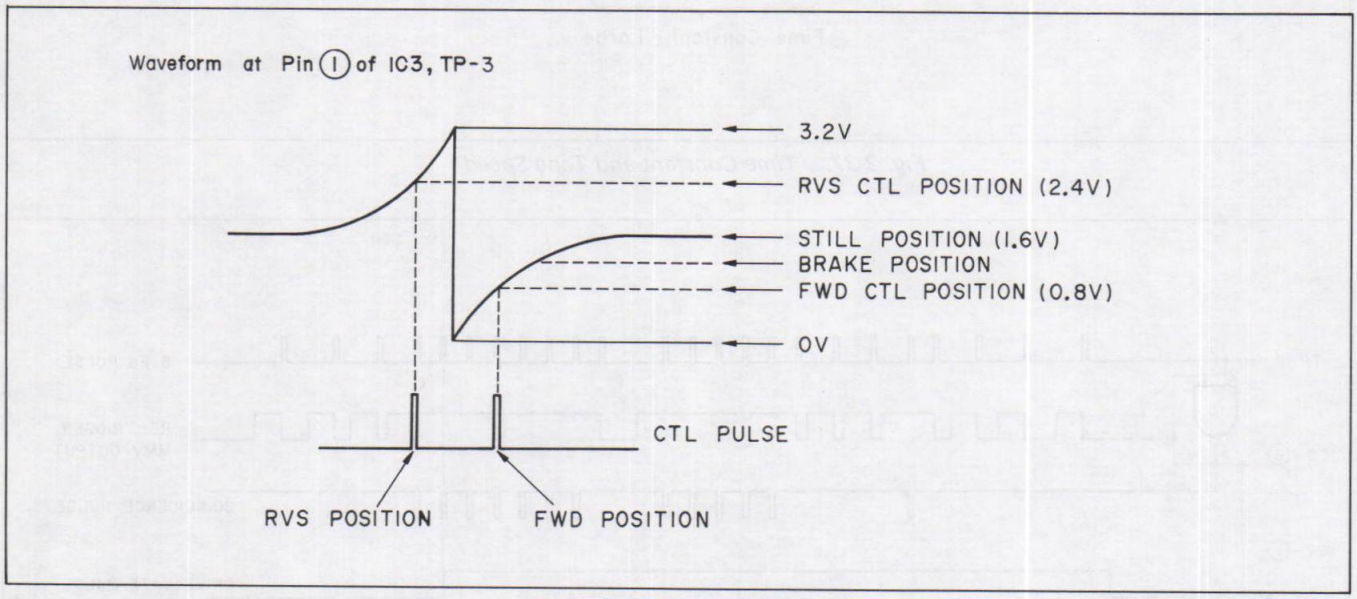


Fig. 3-39. Position Signal

A voltage corresponding to the tape position can be obtained by integrating the 8 FG signal corresponding to the tape speed. The voltage obtained by this integration is called the "POSITION SIGNAL". (See Fig. 3-39)

The center voltage (1.6V) of this POSITION SIGNAL is called the STILL position. Brake gate pulses are generated at the braking position to stop the travelling tape at the STILL position. The POSITION SIGNAL is compensated by the CTL pulse to stop the tape in the STILL position. (See Fig. 3-40) The CTL signal appears early when tape speed increases and appears late when the tape speed decreases. The tape stops at the correct position as the position switch is clamped by the CTL pulse. As the position signal voltage is maintained even where the still position slides after the POSITION SIGNAL is clamped by the CTL pulse, corrections will be made during the next step. Correction will be possible even where one 8 FG pulse is skipped.

The phase errors detected in this manner are fed to the speed PWM circuit in the form of brake gate pulses. Where the STILL time is long, condenser (C7) will leak and it will not be possible to maintain the still position (1.6V). 1.6V is therefore obtained from an external circuit to maintain the STILL position.

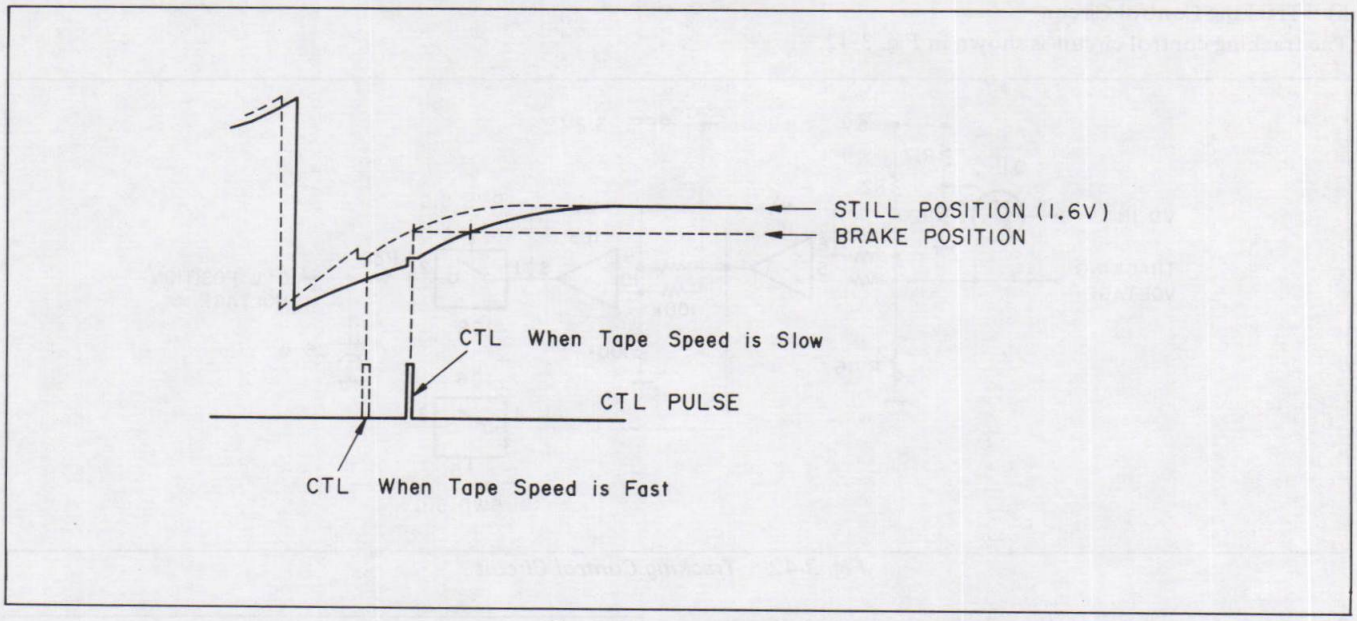


Fig. 3-40. Position Signal

i) CTL Pulse Shaping Circuit

The CTL pulse shaping circuit is shown in Fig. 3-41.
The polarity of the CTL signal is reversed during FWD and RVS. The signal is obtained from the emitter of Q17 during FWD and from the collector of Q17 during RVS. The signals are selected by analog SW IC6 and CTL pulses obtained by waveform shaping in Q18 and IC13, after amplification in IC1.

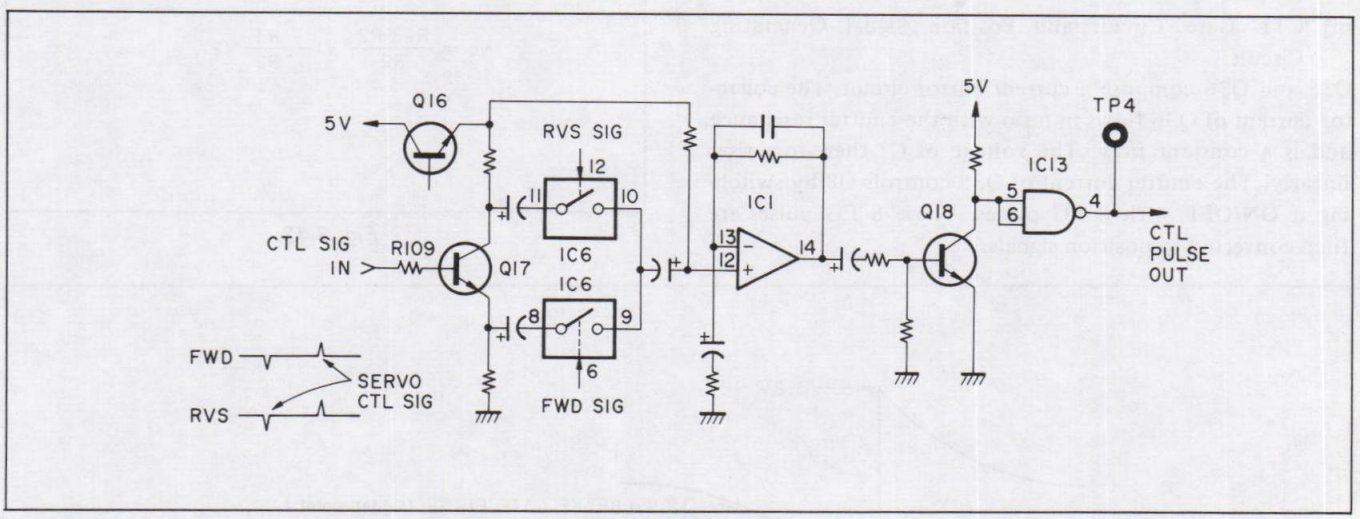


Fig. 3-41. CTL Pulse Shaping Circuit

ii) Tracking Control Circuit

The tracking control circuit is shown in Fig. 3-42.

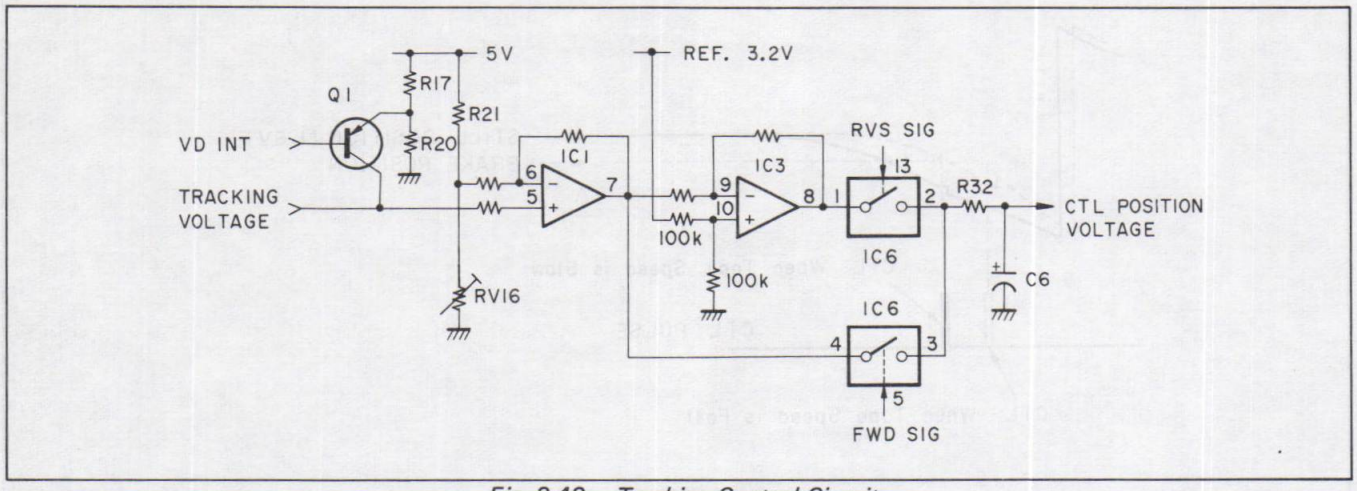


Fig. 3-42. Tracking Control Circuit

The reference voltage of the phase system circuit is the voltage (3.2V) at the midpoint of R48 and R49 and is used as the slow tracking control voltage.

The tracking voltage (Pin 2 of CN4) supplied to Pin 5 (positive side) of IC1 during FWD passes through analog switch IC6 and is memorized in C6 as the CTL position. (The FWD CTL position is about 0.8V) The tracking voltage supplied to pin 5 (positive side) of IC1 during RVS passes through IC3 and analog switch IC6 and is memorized in C6 as the CTL position.

(RVS CTL positon is about 2.4V)

iii) CTL Gate Circuit and Position Signal Generating Circuit

Q35 and Q36 compose a current mirror circuit. The collector current of Q36 flows in ratio with the emitter resistance and is a constant flow. The voltage of C7 there-fore rises linearly. The emitter current of Q35 controls Q8 by switching it ON/OFF with 8 FG pulses. These 8 FG pulses are then converted to position signals.

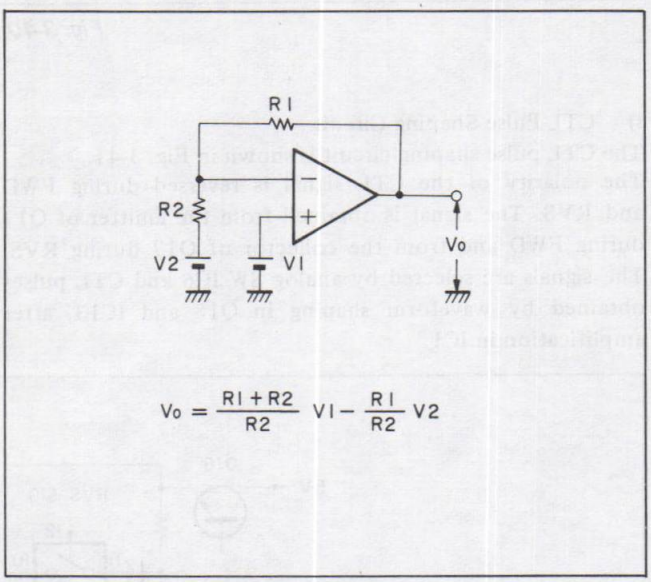


Fig. 3-43.

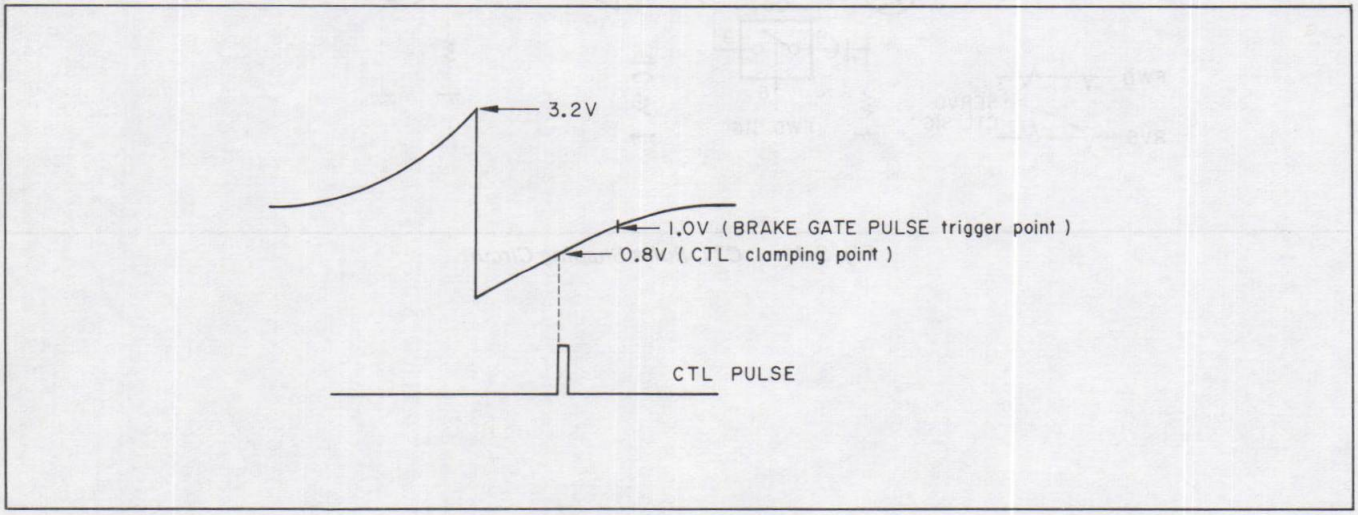


Fig. 3-44. Position Signal

The angle of the POSITION SIGNAL is controlled by RV2 and is clamped at 0.8V with the CTL pulse. IC3 is a buffer and the POSITION SIGNAL appears as an output at TP3. IC3 is for detecting the 3.2V level of the POSITION SIGNAL and, when TP3 reaches 3.2V, outputs signals to turn Q9 ON and drop TP3 voltage to 0V.

IC3 is a comparator (forming a Schmitt circuit by positive feedback) to detect brake position and uses RV4 to adjust brake position (set to approx. 1V) and subsequently triggers brake gate pulses.

Q3 and Q4 are analog switches controlled by CTL pulses and, from the relation C6 ⩾ C7, the voltage of C7 is instantaneously clamped to the tracking voltage.

Q10 is a switch that locks the POSITION SIGNAL in STILL position (1.6V) when the STILL time is over 8 seconds. It is triggered by IC10 (time constant R92, C27) after waveform is shaped and is reset by Q25. Q25 is controlled by drive gate pulses and the $\overline{\text{SLOW}}$ signal.

Where the slow servo is locked in a position where CTL signals are not obtainable during the $\overline{\text{SLOW}}$ mode, the POSITION SIGNAL cannot be clamped by CTL pulses as there will be no CTL signals even where the tracking knob is turned.

When the tracking knob is turned, C3 and C44 change the reference voltage (Pin 6 of IC3) determining the braking position and thus shift the brake timing to release the lock.

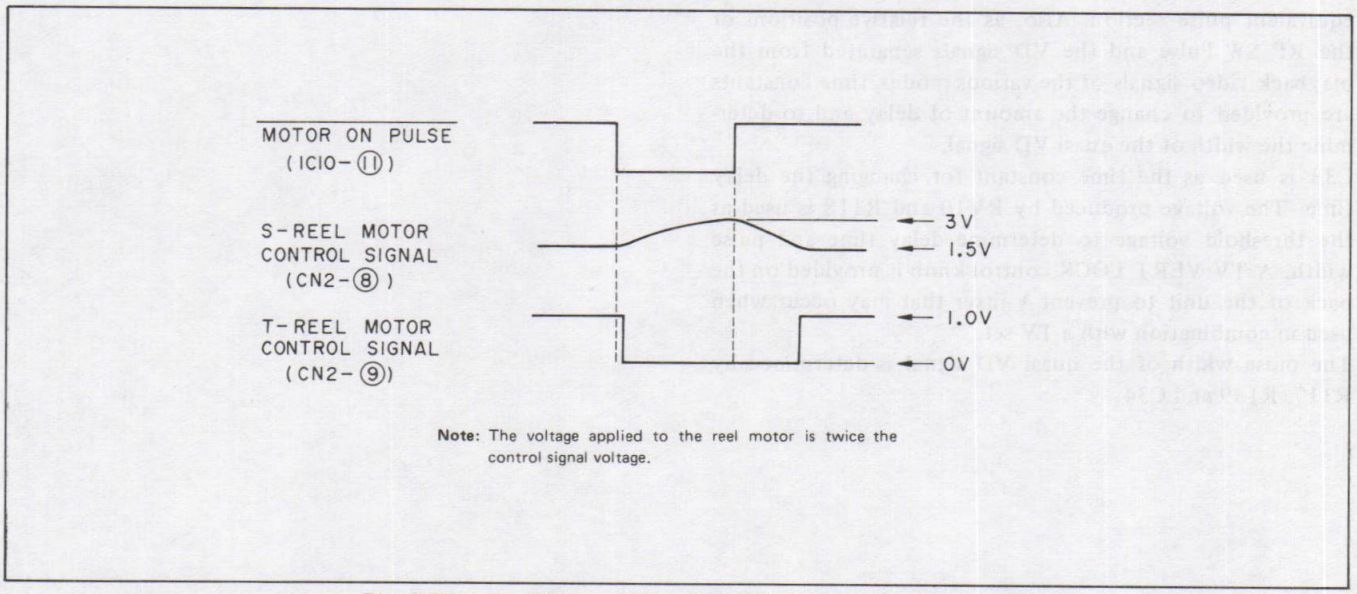
3-3-2. Tape Tension Control and Reel Correction

Tape tension is controlled by the S-reel motor and the T-reel motor. Control during CUE and REV modes is carried out by the reel circuit contained in SS-11 board and control during the RVS mode is carried out by JR-1 board.

When the tape is stopped in the STILL, X1RVS mode, 3V (the voltage across the reel motor terminals is set at twice the control signal voltage) is applied to obtain the necessary tape tension.

A voltage of 2V is applied to the T-reel motor to prevent slack from developing in the tape. On one hand, 6V is applied to the S-reel motor while the tape is travelling during the RVS slow mode to take up the tape and the T-reel motor is maintained at 0.5V (called tension killer).

On the S-reel motor side, 1.5V is obtained from R129 and R130, Q22 is turned ON by $\overline{\text{MOTOR ON PULSES}}$ while the tape is travelling and its emitter voltage integrated by C41 to produce the S-reel motor control signal, shown in Fig. 15. On the T-reel motor side, 1V is obtained from R123 and R124 and, while the tape is in motion, the $\overline{\text{MOTOR ON PULSE}}$ (Pin 10 of IC10) is delayed by C38 and 4.7kΩ and Q6 is turned ON to effect tension killing.



Note: The voltage applied to the reel motor is twice the control signal voltage.

Fig. 3-45. Reel Motor Control Signals During Step Feed

3-3-3. JOG Control System

The JOG control circuit is contained in IC5 and is used for insertion of quasi VD signals and generation of head switching signals.

1) Quasi VD Signal Insertion Circuit

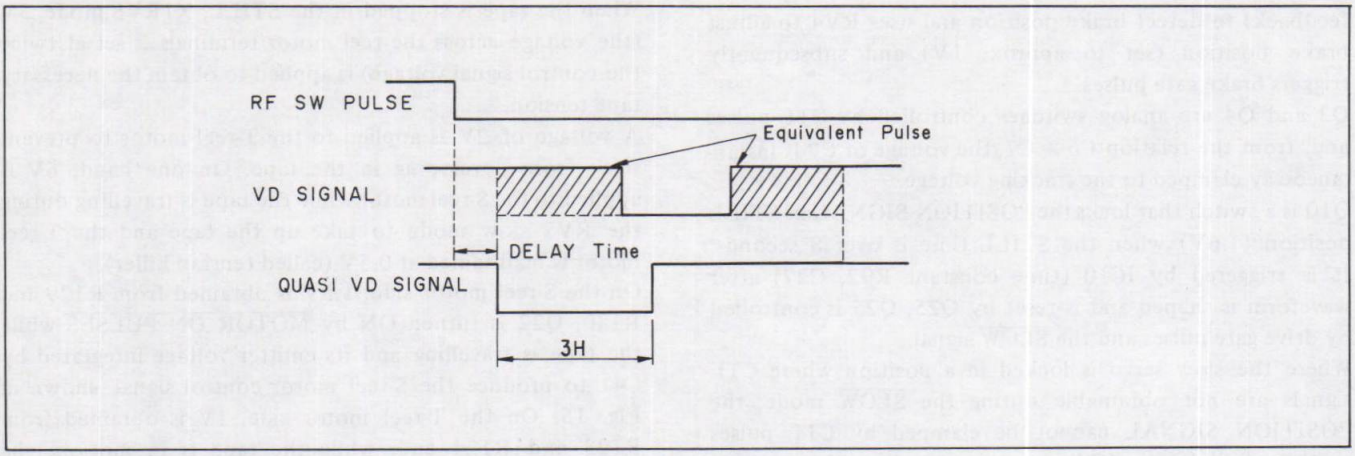


Fig. 3-46. Quasi Video Signal

This circuit operates when the JOG signal is high ("H"). The quasi VD signal is produced by delaying the RF SW pulse and is inserted for a 3H portion including the equivalent pulse section. Also, as the relative positions of the RF SW Pulse and the VD signals separated from the playback video signals of the various modes, time constants are provided to change the amount of delay and to determine the width of the quasi VD signal.

C33 is used as the time constant for changing the delay time. The voltage produced by RV10 and R118 is used as the threshold voltage to determine delay time and pulse width. A TV VERT LOCK control knob is provided on the back of the unit to prevent V-jitter that may occur when used in combination with a TV set.

The pulse width of the quasi VD signal is determined by R117, R139 and C34.

2) Head Switching Signal –A', B

RVN	SLOW	JOG	HEAD	MODE
—	—	L	B	x 1
H	L	H	B	C/R, –1
L	L	H	A'	x 2
—	H	H	A'	SLOW STILL
—	H	H	B	SLOW TRANSIET (STILL → x1)

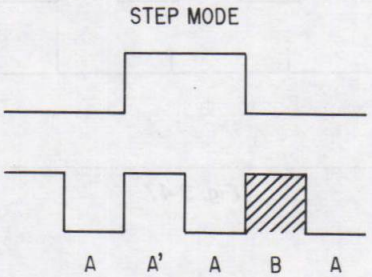


Table 3-5.

MODE	VPG (IC5– ⑰)
STILL, X2 FWD	LOW
X1 FWD, X1 RVS, SPEED SEARCH	RF SW PULSE
STEP	(RF SW PULSE A B) VPG

Table 3-6.

The head switching signal is formed from the RF SW pulses. The outputs from the various modes are shown in Table 3-6.

3-3-4. Editing System

When switching from the slow mode variable speed playback to the servo variable speed playback mode, the capstan servo can be locked early by timing the CAP CUT signal with the RF SW pulse. (See Fig. 3-47)

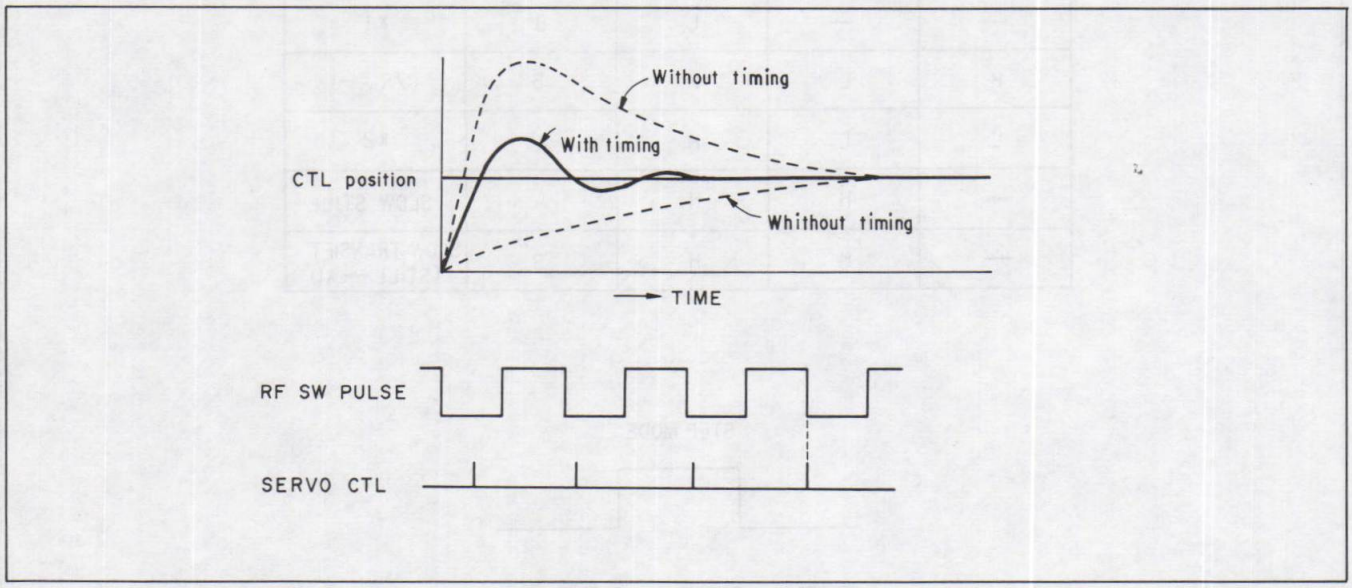


Fig. 3-47.

The editing circuit determines the falling position of the CAP CUT signal and determines this position by means of RV6. RV6 compares the CTL signal with the RF SW pulse and makes any necessary adjustments to bring the CTL signal to its correct position within the 8 CTLs.

When the SLOW signal (Pin 13 of IC7) becomes high, it passes through D2 and causes the CAP CUT signal to rise. When Pin 13 of IC7 becomes low, C24 will be discharged through RV6 and cause the CAP CUT signal to fall. (See Fig. 3-48)

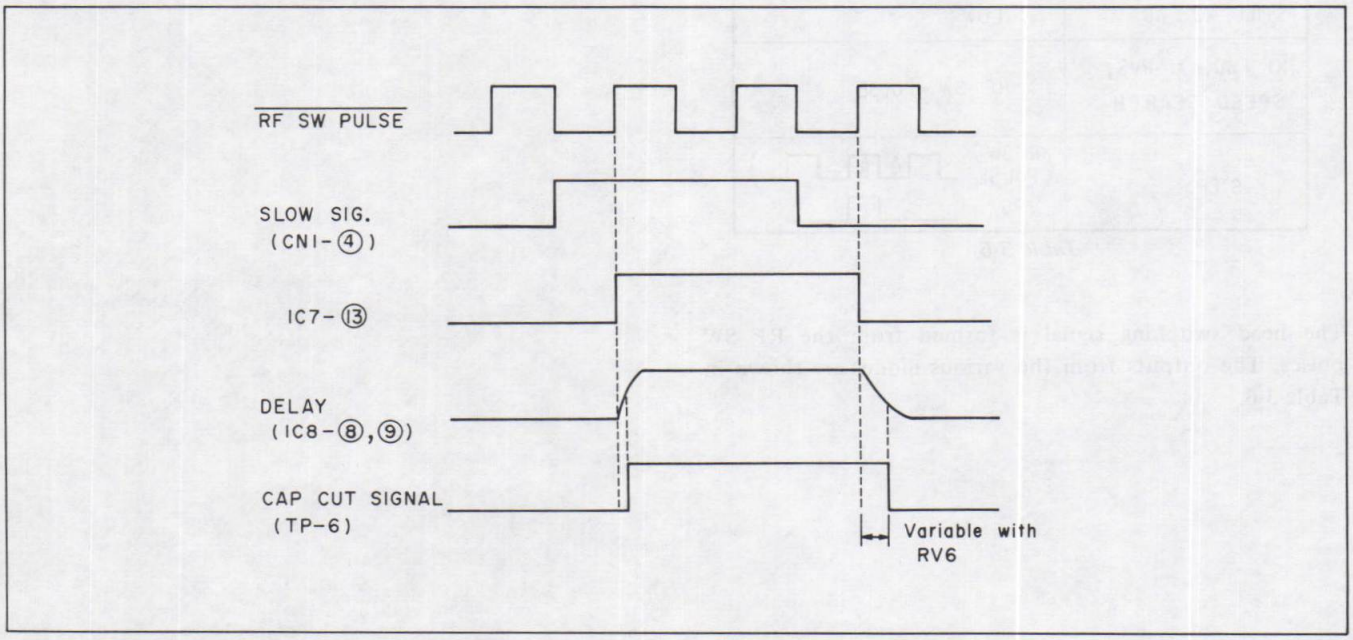


Fig. 3-48. Edit Timing Chart

3-3-5. Drum Compensation Circuit

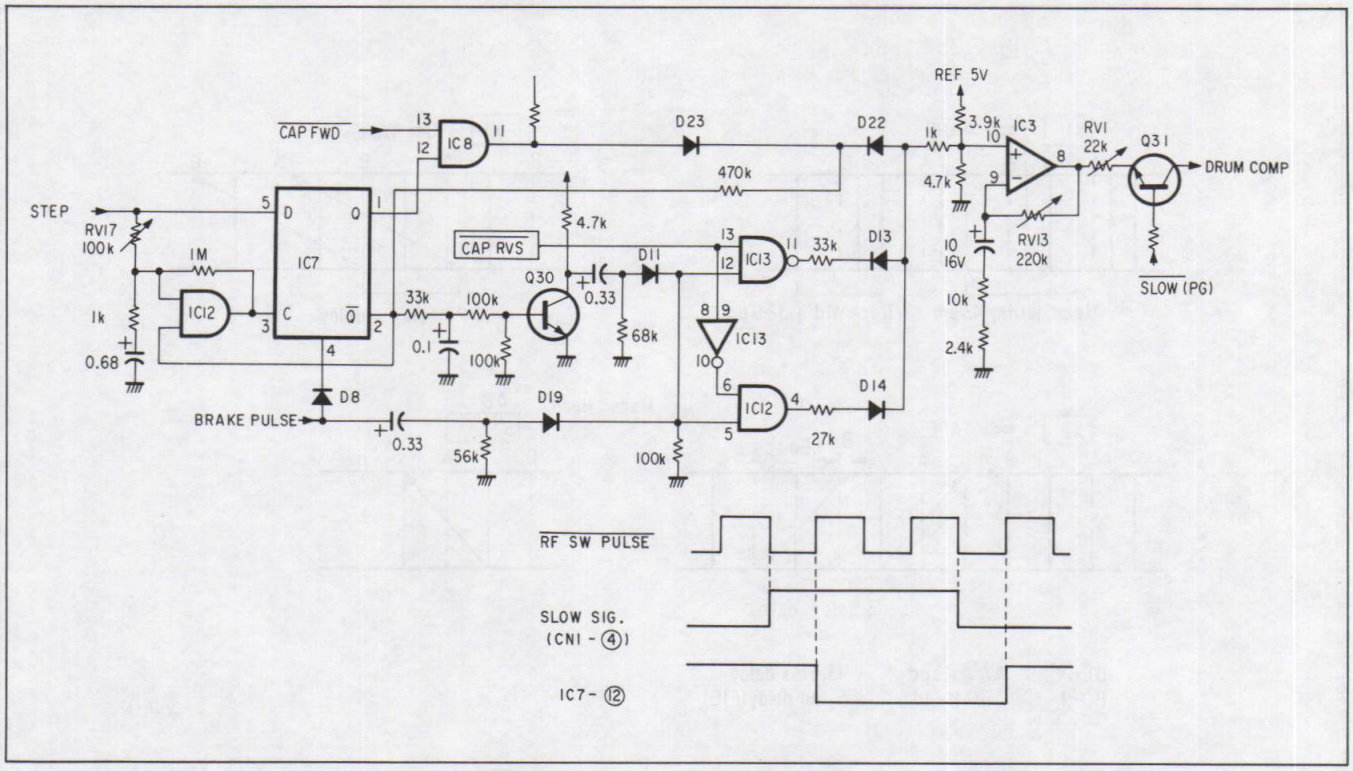


Fig. 3-49.

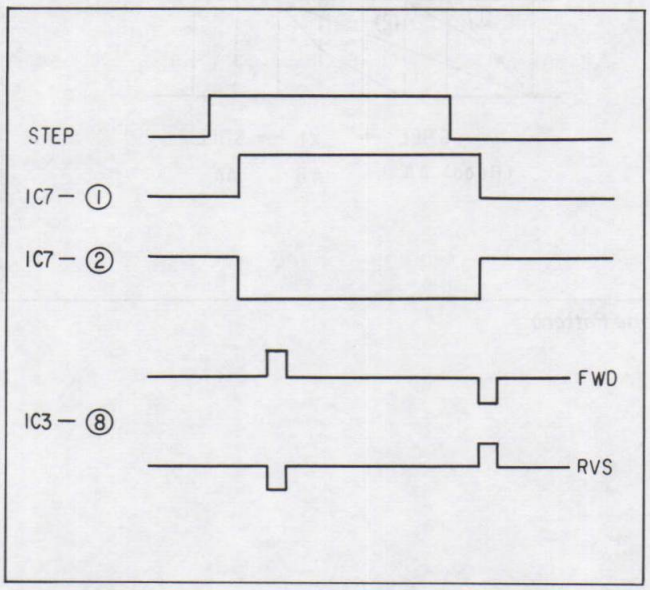


Fig. 3-50.

The signal on Pin 1 of IC7 is produced from STEP signals and step DELAY signal. It rises equivalent to the amount of delay of 33K, 0.1μ of Pin 2 of IC7 and produces positive compensation pulses during FWD operation. This positive compensation pulse is fed to Pin 10 of IC3 and appears as an output at Pin 8 of IC3. It is controlled so that outputs are available only during slow operation. This signal is fed to the normal system for drum compensation and to carry out fH correction in CUE and REV modes. Similarly, the reverse compensation voltage synchronized with the rise of Pin 2 of IC7 is fed to the drum loop of the normal servo. $\overline{\text{CAP RVS}}$ are synthesized on Pin 12 of IC13 and become drum compensation voltages during FWD operation. Pin 12 of IC13 becomes reversed in direction during RVS causing $\overline{\text{CAP RVS}}$ to also become reversed.

The trace angle of the video head and tape pattern normally differ during playback and STILL periods. For this reason, the horizontal frequency shifts approximately 0.3% during STILL operation. The drum shift circuit functions to compensate for this shift by supplying a compensating voltage to the drum speed system circuit contained in the JR-1 PC Board. Compensation is carried out during STILL periods by supplying DC elements and, during tape feed, by applying $\overline{\text{MOTOR ON PULSES}}$ and BRAKE GATE PULSES. Direction of compensation will be reversed in the case of the FWD mode and RVS mode.

3-3-6. Others

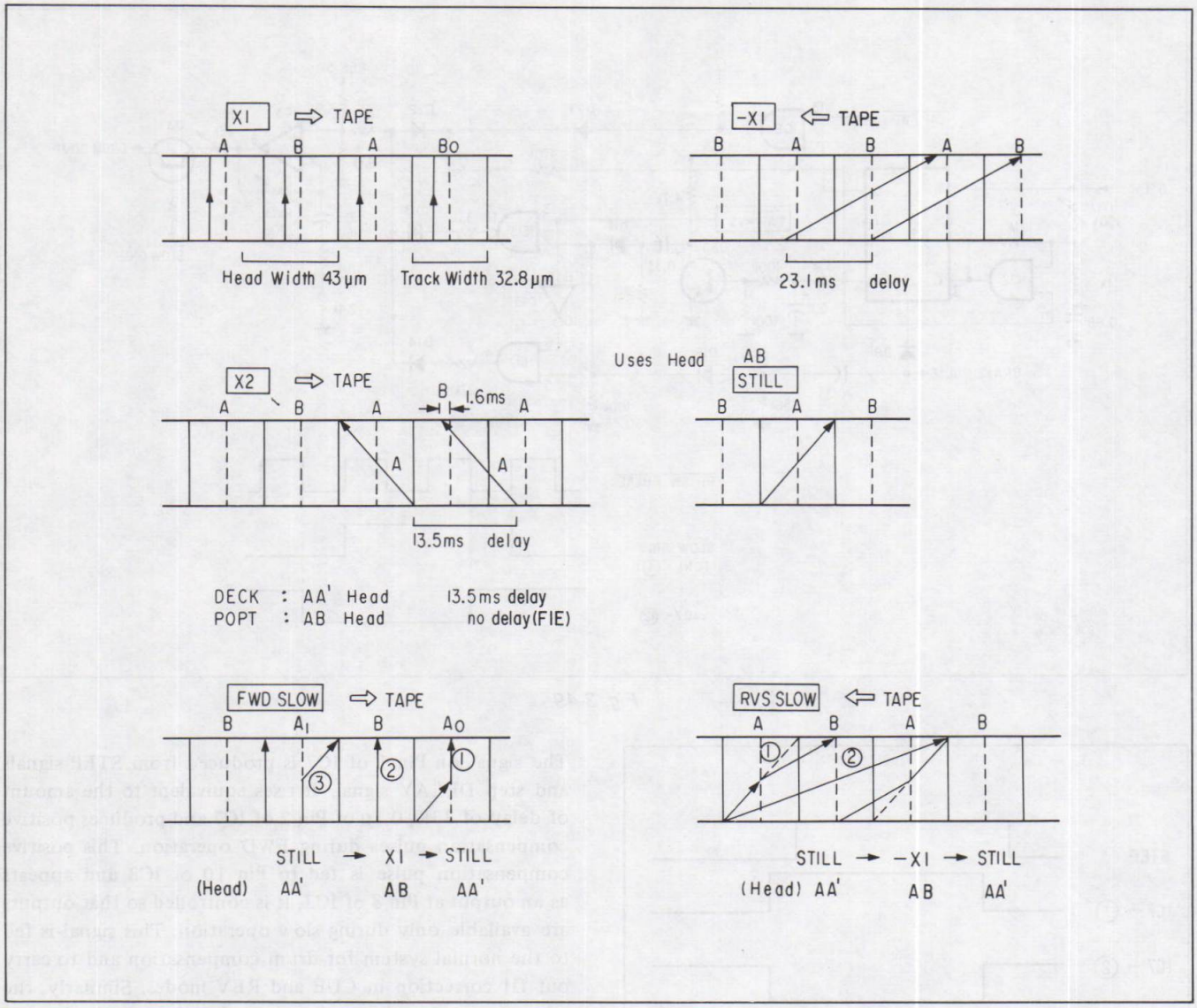


Fig. 3-51. Tape Pattern

SECTION 4
POWER CIRCUIT

The power circuit block diagram and timing chart are shown in Figures 4-1 and 4-2, respectively.

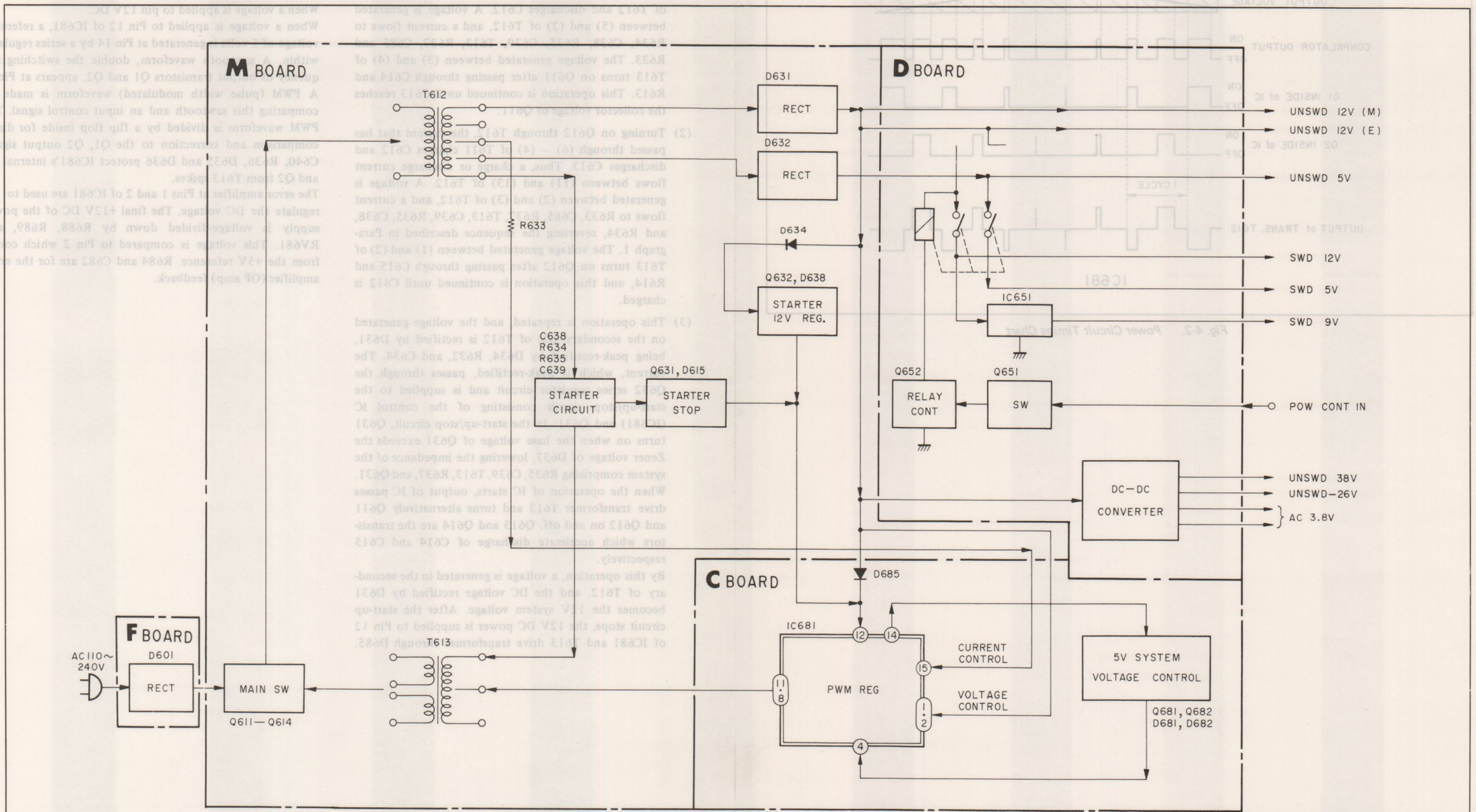


Fig. 4-1. Power Circuit Block Diagram

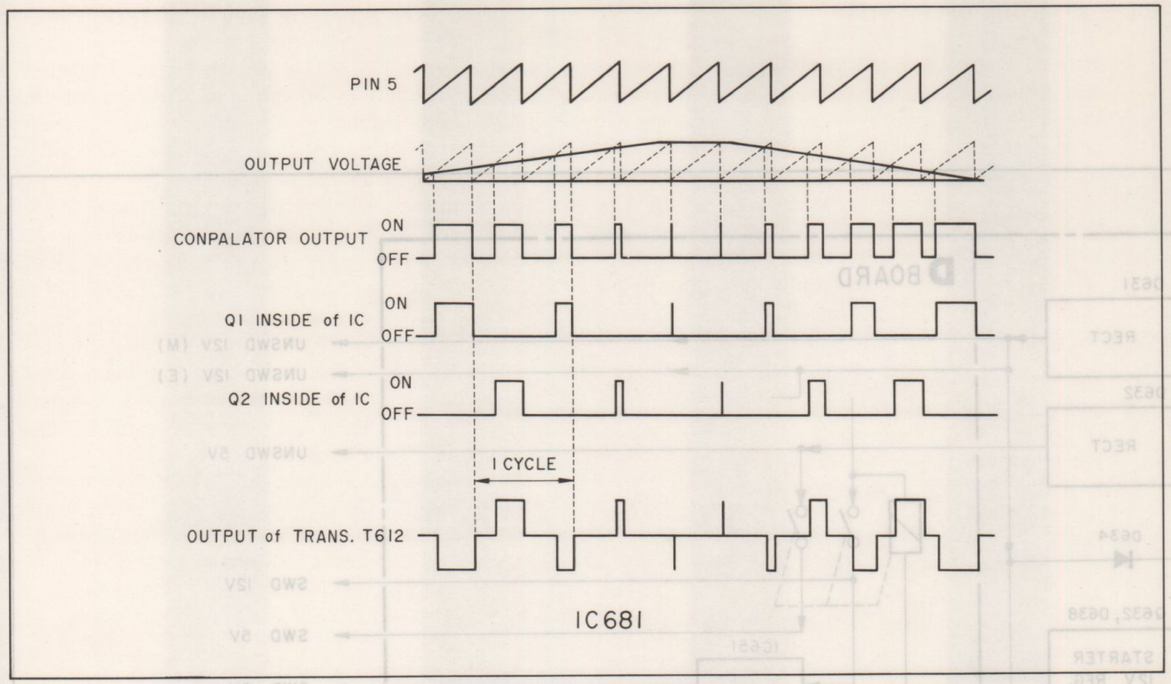


Fig. 4-2. Power Circuit Timing Chart

4-1. START-UP OPERATION

(1) Turning on the ON/STANDBY switch S601, the current rectified by D601 turns on Q611 after passing through (6) – (4) of T611. The current charges C613 after passing from the emitter of Q611 to (13) – (11) of T612 and discharges C612. A voltage is generated between (5) and (2) of T612, and a current flows to R634, C638, R635, C639, T613, R637, C685 and R633. The voltage generated between (3) and (4) of T613 turns on Q611 after passing through C614 and R613. This operation is continued until C613 reaches the collector voltage of Q611.

(2) Turning on Q612 through T612, the current that has passed through (6) – (4) of T611 charges C612 and discharges C613. Thus, a charge or discharge current flows between (11) and (13) of T612. A voltage is generated between (2) and (3) of T612, and a current flows to R633, C685, R637, T613, C639, R635, C638, and R634, reversing the sequence described in Paragraph 1. The voltage generated between (1) and (2) of T613 turns on Q612 after passing through C615 and R614, and this operation is continued until C612 is charged.

(3) This operation is repeated, and the voltage generated on the secondary side of T612 is rectified by D631, being peak-rectified by D634, R632, and C634. The current, which is peak-rectified, passes through the Q632 series regulator circuit and is supplied to the start-up/stop circuit consisting of the control IC (IC681) and Q631. In the start-up/stop circuit, Q631 turns on when the base voltage of Q631 exceeds the Zener voltage of D637, lowering the impedance of the system comprising R635, C639, T613, R637, and Q631. When the operation of IC starts, output of IC passes drive transformer T613 and turns alternatively Q611 and Q612 on and off. Q613 and Q614 are the transistors which accelerate discharge of C614 and C615 respectively.
By this operation, a voltage is generated in the secondary of T612, and the DC voltage rectified by D631 becomes the 12V system voltage. After the start-up circuit stops, the 12V DC power is supplied to Pin 12 of IC681 and T613 drive transformer through D685.

4-2. OUTPUT VOLTAGE (12V) CONTROL CIRCUIT

Control of the 12V DC supplies is achieved by changing the pulse width (duty cycle) output of IC681. Voltage regulation, current limiting, and shutdown are also controlled in the circuit below.
When a voltage is applied to pin 12V DC.
When a voltage is applied to Pin 12 of IC681, a reference voltage of 5 volts is generated at Pin 14 by a series regulator within. A sawtooth waveform, double the switching frequency of output transistors Q1 and Q2, appears at Pin 5. A PWM (pulse width modulated) waveform is made by comparing this sawtooth and an input control signal. The PWM waveform is divided by a flip flop inside for direct comparison and correction to the Q1, Q2 output signal. C640, R636, D635 and D636 protect IC681's internal Q1 and Q2 from T613 spikes.
The error amplifier at Pins 1 and 2 of IC681 are used to regulate the DC voltage. The final +12V DC of the power supply is voltage-divided down by R688, R689, and RV681. This voltage is compared to Pin 2 which comes from the +5V reference. R684 and C682 are for the error amplifier (OP amp) feedback.

4-3. PROTECTION CIRCUIT

(1) Over current protection
All the output current is detected by 0.02Ω R633 and controlled by error amplifier IC681. Setting has been made so that "フ" shape overcurrent protection is applied at 10A to 12A. (Setting may be changed R686 and R687.)

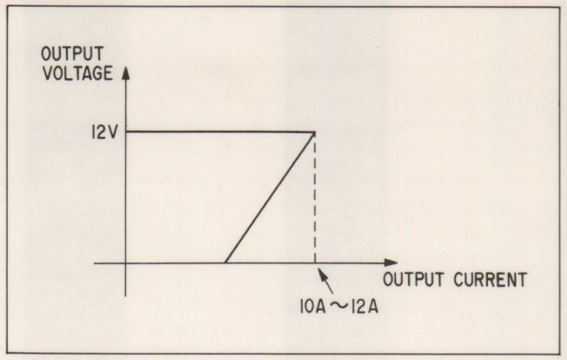


Fig. 4-3.

(2) Over-voltage Protection
i) 12V System
The 13V Zener diode D683 turns on to pull up the voltage on Pin 4 of IC681 and to lower the output voltage when the 12V system voltage exceeds 15V.
ii) 5V System
The 5.6V Zener diode D682 turns on to pull up the voltage on Pin 4 of IC681 and lowers the output voltage when the 5V system voltage exceeds 8V.

(3) Power protection in proportion to input voltage
When input voltage is controlled in constant value. Therefore, voltage which has been peak-rectified by D634, R632 and C634 is impressed on Pin 4 of IC681 through R695 and D684.
Thus, power is controlled so that an increase in duty does not exceed a certain value when the input voltage is high.

(4) Short-circuit Protection
Q682 and Q681 turn on to pull up the voltage on Pin 4 of IC681 and lowers the output voltage when the 5V system voltage lowers.

4-4. SCHEMATIC DIAGRAM

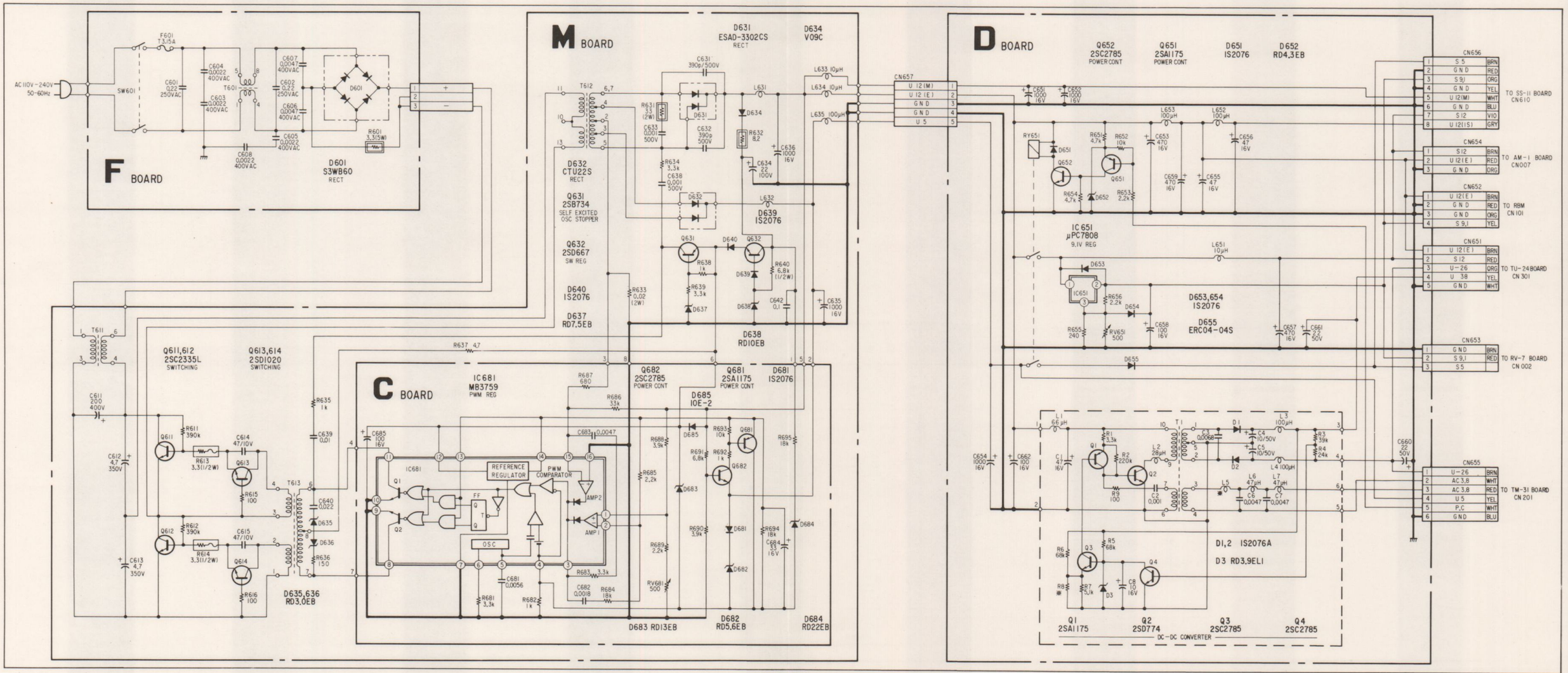


Fig. 4-4.

SECTION 5
AUDIO CIRCUIT

Channel 2, is shown in parentheses ( ).

5-1. INPUT SELECTION CIRCUIT (AM-1 AND HM-1 BOARDS)

Both Channels 1 and 2 have line, camera, and mic inputs as voice inputs. The tuner input signal is input to Pin 12 (Pin 1) of IC501, the line input signal, to Pin 14 (Pin 5), and the camera input signal, to Pin 15 (Pin 2). These signals are selected by the LINE SELECT and CAMERA SELECT signals and are output from Pin 13 (Pin 3).

PIN 9 (CAMERA SELECT)	PIN 10 (LINE SELECT)	PIN 3, PIN 13 OUTPUT SIGNALS
L	L	Tuner Input
H	L	Camera Input
L	H	Line Input

Table 5-1.

The output from Pin 13 (Pin 3) of IC501 is input in the buffer Q601 (Q602) through the mic jack on the HM-1 Board. Mic signals are input in Q601 (Q602) on a priority basis when the mic is used.

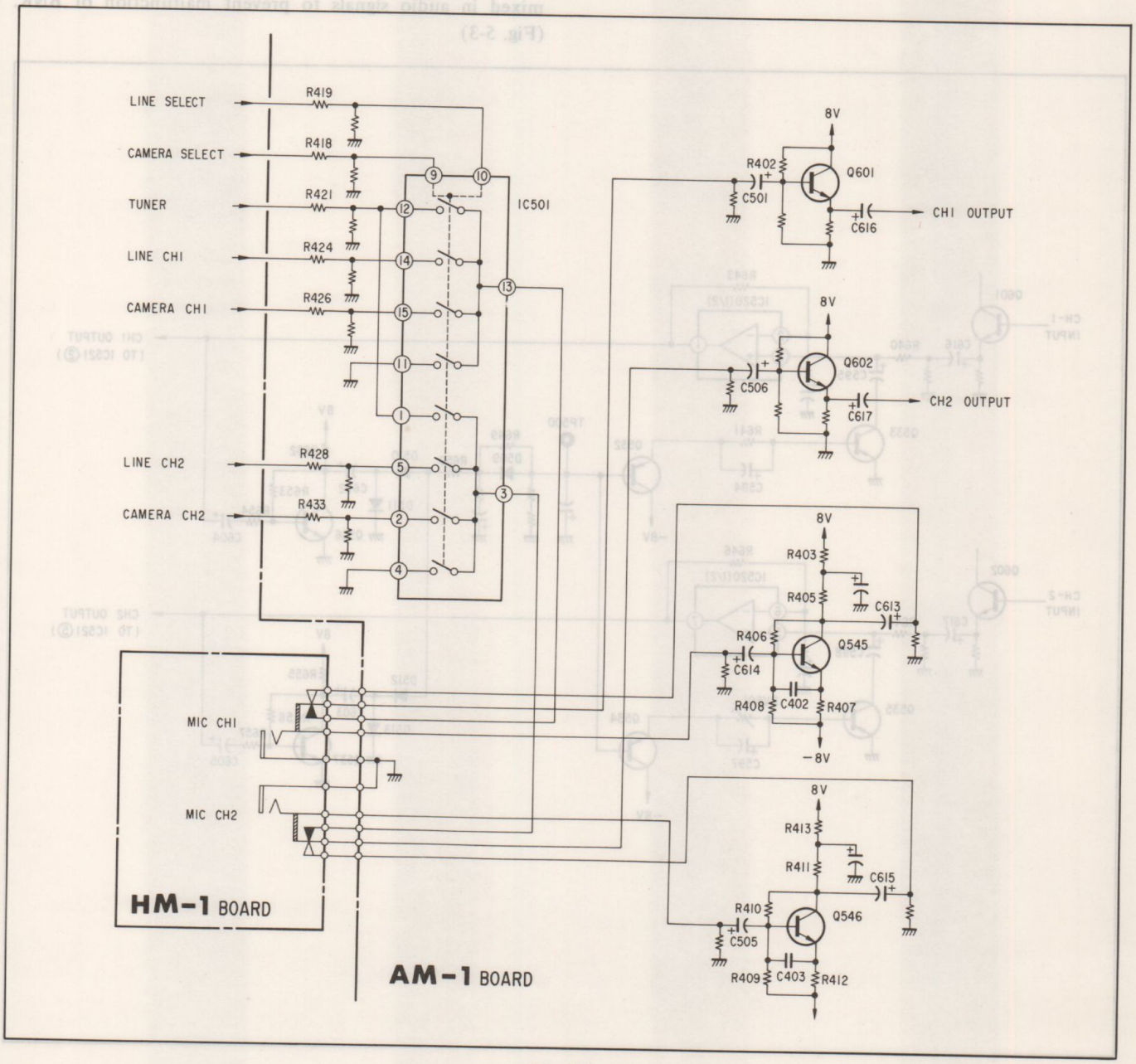


Fig. 5-1.

5-2. AGC CIRCUIT (AM-1 BOARD)

The signals passing through the buffer Q601 (Q602) are input to Pin 2 (Pin 5) of the RECORD/PLAYBACK selector switch IC521 after passing through the AGC circuit comprising IC520, Q536, Q532, and Q533 (IC520, Q537, Q534, and Q535). The automatic gain control is performed as follows. The output of Pin 1 (Pin 7) of IC520 is rectified by D510 and D511 (D512 and D513) and charged to C600 after being amplified by Q536 (Q537). The voltage charged in C600 controls the resistance value between the collector and emitter of Q533 (Q535), as well as the input level of Pin 3 (Pin 5) of IC520.

5-3. RECORD/PLAYBACK SELECTOR CIRCUIT (AM-1 BOARD)

The audio signals from the AGC circuit are input in Pin 2 (Pin 5) of IC521. The PB CH1 signals (PB CH2 signals) are impressed to Pin 10 (Pin 9) of IC521. In the PLAYBACK mode or in the AUDIO DUB CH2 mode, the level of PB CH1 signals becomes "H". The level of PB CH2 signals becomes "H" only in the "PLAYBACK" mode. (Table 5-4)

In the RECORD mode, the level of Pin 10 (Pin 9) of IC521 is L, and the Pin 2 (Pin 5) input is output to Pin 15 (Pin 4). The audio signal outputs of Pin 15 (Pin 4) are input from the emitter of Q541 (Q542) to the BNR switch IC506 (IC508) through LPF T505 (T506). The LPF removes the horizontal synchronizing and recording bias signals mixed in audio signals to prevent malfunction of BNR. (Fig. 5-3)

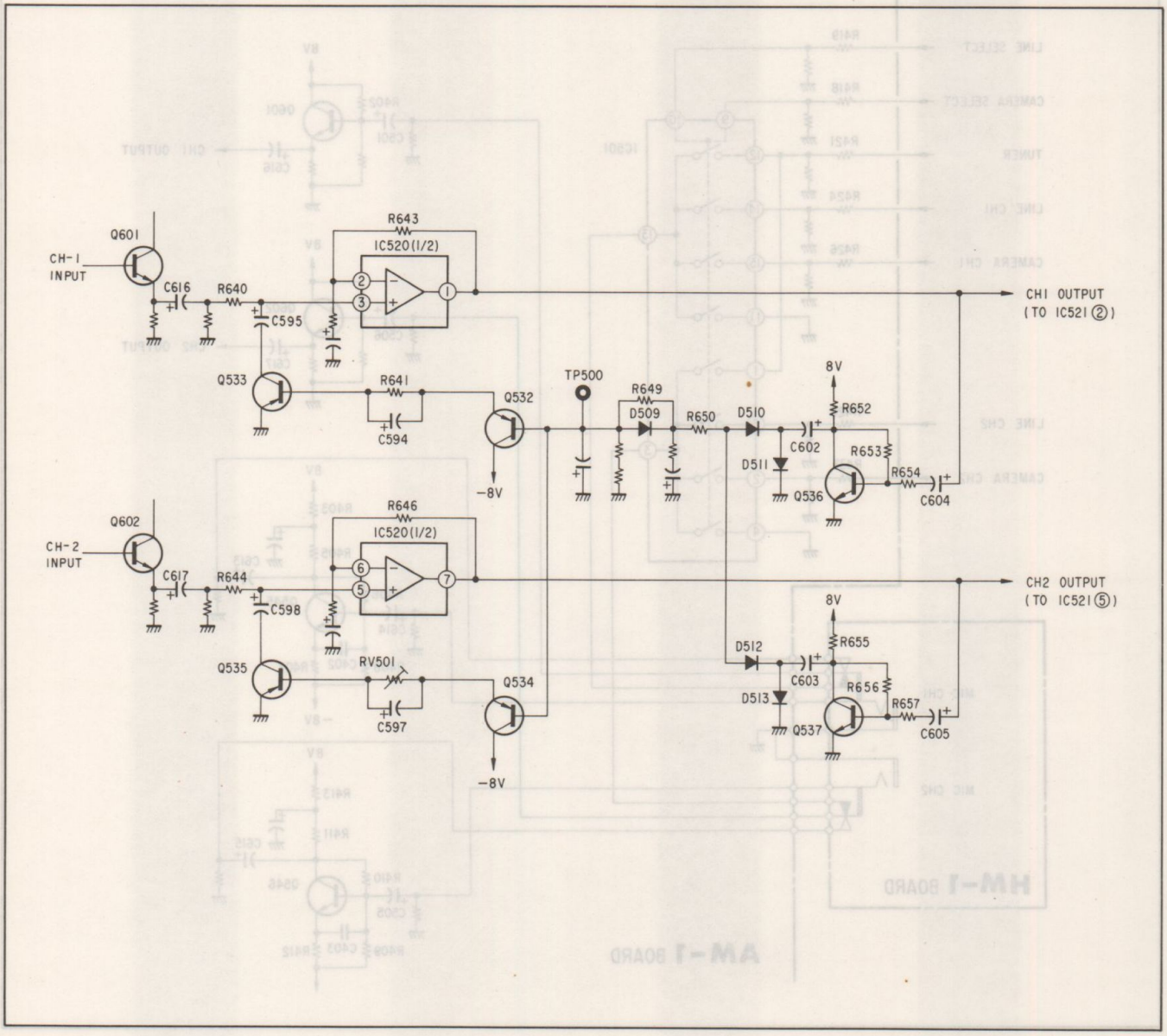


Fig. 5-2.

5-4. BNR CIRCUIT (AM-1 BOARD)

The BNR circuit operation is switched by the BNR switch IC506 (IC508). This IC is controlled by the voltages of Pins 9, 10, and 11. (Fig. 5-3 and Table 5-2)

BNR	MODE	PIN 9	PIN 10	PIN 11
ON	REC/E-E	L	L	H
	PB	H	H	L
OFF	REC/E-E	L	L	L
	PB	L	L	L

Table 5-2.

1) BNR OFF MODE

Inside the BNR switch IC506 (IC508), Pins 12 and 14, Pins 2 and 15, and Pins 5 and 4 are connected. For this reason, the output of Q541 (Q542) is output to the recording circuit through Pins 12 and 14 of IC506 and to the monitor output circuit through Pins 5 and 4 of IC506, as it is.
At that time, Q512 (Q504) is turned OFF, a negative feedback is applied from Pin 7 to Pin 6 of IC509 (IC510) through R563 and R564 (R528 and R529), and the loop gain of IC509 (IC510) is lowered. (Fig. 5-3.)

2) BNR ON RECORD/E-E MODE

Inside the BNR switch IC506 (IC508), Pins 13 and 14, and Pins 2 and 15, and Pins 5 and 4 are connected. For this reason, the output signal of Q541 (Q542) is output to the monitor output circuit through Pins 5 and 4 of IC506 (IC508) as it is. However, the output to the RECORD circuit is output after being BNR-encoded. The output signal of Q541 (Q542) is input to Pin 11 (Pin 6) of IC507 through Pins 5 and 4 of IC506 (IC508) and through C529 and R547 (C524 and R536) and is output from Pin 10 (Pin 7) after being inversion-amplified in the IC. The inverted amplifier is applied with a variable negative feedback through variable gain cells inside Pins 2 and 15 of IC506 (IC508), C530 (C523), and inside Pin 14 (Pin 3) of IC507. The amplifier functions as a BNR compressor. The output of Pin 10 (Pin 7) of IC507 is input to Pin 6 of IC509 (IC510) through Pins 2 and 15 of IC506 (IC508) and through R561 (R525). At that time, the output of Pin 4 of IC506 (IC508) is also input to Pin 6 through C538 and R560 (C517 and R526). Both are in an antiphase relationship, and the latter is subtracted from the former. The signal input to Pin 6 of IC509 (IC510) is output to the RECORD circuit from Pin 7 after passing through Pins 13 and 14 of IC506. A negative feedback is applied from Pin 7 to Pin 6 of IC509 (IC510) through Pins 13 and 14 of IC506 and through C536, R557, and R559 (C515, R522, and R524), to perform a fixed pre-emphasis. The encoder output from Pin 14 of IC506 is input in a weighting circuit made up of IC509, C534, C535, R568, R569, and RV505 (IC510, C518, C519, R531, R532, and RV502) and is output from Pin 1 of IC509 (IC510). The output is input in Pin 15 (Pin 2) of IC507, is rectified, is charged to C531 at Pin 16 (C522 of Pin 1), and is applied to the variable gain cell to control the gain. Q507, Q508, and RV504 (Q505, Q506, and RV503) of Pin 16 (Pin 1) of IC507 limits the control voltage of the variable gain cell.
Q512 (Q504) is turned ON and the loop gain of IC509 (IC510) is increased.

3) BNR ON PLAYBACK MODE

Inside the BNR switch IC506 (IC508), Pins 12 and 14, Pins 1 and 15, and Pins 3 and 4 are connected. For this reason, the output of Q541 (Q542) is BNR-decorded and is output to the monitor circuit.
The output of Q541 (Q542) is input to Pin 6 of IC509 (IC510) after passing through Pins 12 and 14 of IC506 (IC508) and the fixed deemphasis circuit consisting of C536, C537, R557, R558, and R559 (C525, C516, R522, R523, and R524). At that time, the decoder output of Pin 4 of IC506 (IC508) is added to this input signal through C538 and R560 (C517 and R526). The output of Pin 7 of IC509 (IC510) is input to Pin 14 (Pin 3) of IC507 after passing through Pins 1 and 15 of IC506 (IC508) and through C530 (C523). The signal is output from Pin 10 (Pin 7) of IC507 via the variable gain cell and expanded inverted amplifier. The output signal is output to the monitor output circuit through Pins 3 and 4 of IC506 (IC508). The output from Pin 14 of IC506 (IC508) is input to Pin 15 (Pin 2) of IC507 through the weighting circuit comprising IC509, C534, C535, R568, and R569 (IC510, C518, C519, R531, and R532) to control the gain of the variable gain cell. Q512 (Q504) turns on to increase the loop gain of IC509 (IC510).

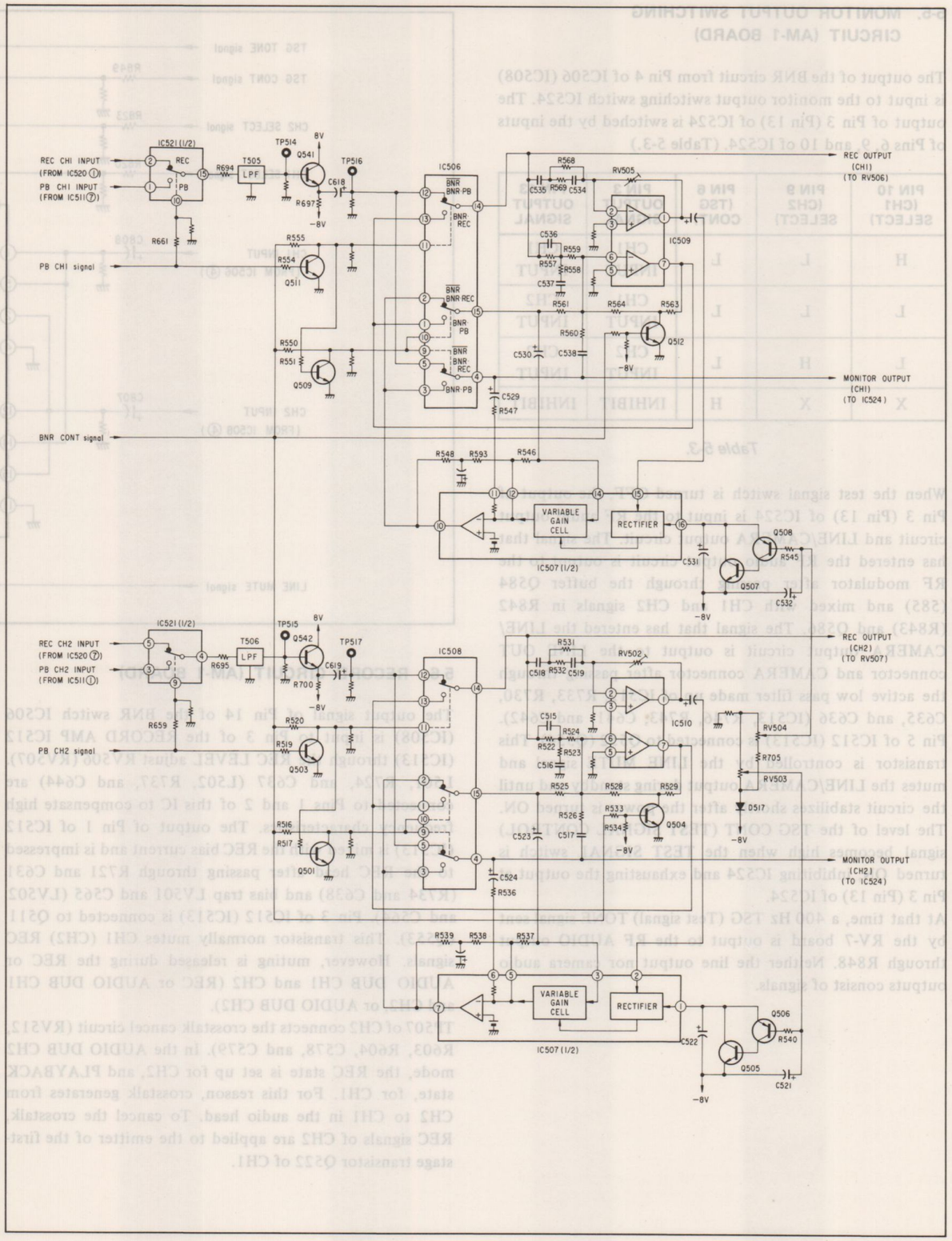


Fig. 5-3.

5-5. MONITOR OUTPUT SWITCHING CIRCUIT (AM-1 BOARD)

The output of the BNR circuit from Pin 4 of IC506 (IC508) is input to the monitor output switching switch IC524. The output of Pin 3 (Pin 13) of IC524 is switched by the inputs of Pins 6, 9, and 10 of IC524. (Table 5-3.)

PIN 10 (CH1 SELECT)	PIN 9 (CH2 SELECT)	PIN 6 (TSG CONT)	PIN 3 OUTPUT SIGNAL	PIN 13 OUTPUT SIGNAL
H	L	L	CH1 INPUT	CH1 INPUT
L	L	L	CH1 INPUT	CH2 INPUT
L	H	L	CH2 INPUT	CH2 INPUT
X	X	H	INHIBIT	INHIBIT

Table 5-3.

When the test signal switch is turned OFF, the output of Pin 3 (Pin 13) of IC524 is input to the RF audio output circuit and LINE/CAMERA output circuit. The signal that has entered the RF audio output circuit is output to the RF modulator after passing through the buffer Q584 (585) and mixed with CH1 and CH2 signals in R842 (R843) and Q586. The signal that has entered the LINE/CAMERA output circuit is output to the LINE OUT connector and CAMERA connector after passing through the active low pass filter made up of IC512, R733, R730, C635, and C636 (IC513, R746, R743, C641, and C642). Pin 5 of IC512 (IC513) is connected to Q552 (Q554). This transistor is controlled by the LINE MUTE signal and mutes the LINE/CAMERA output during standby and until the circuit stabilizes shortly after the power is turned ON. The level of the TSG CONT (TEST SIGNAL CONTROL) signal becomes high when the TEST SIGNAL switch is turned ON, inhibiting IC524 and exhausting the output at Pin 3 (Pin 13) of IC524.

At that time, a 400 Hz TSG (Test signal) TONE signal sent by the RV-7 board is output to the RF AUDIO output through R848. Neither the line output nor camera audio outputs consist of signals.

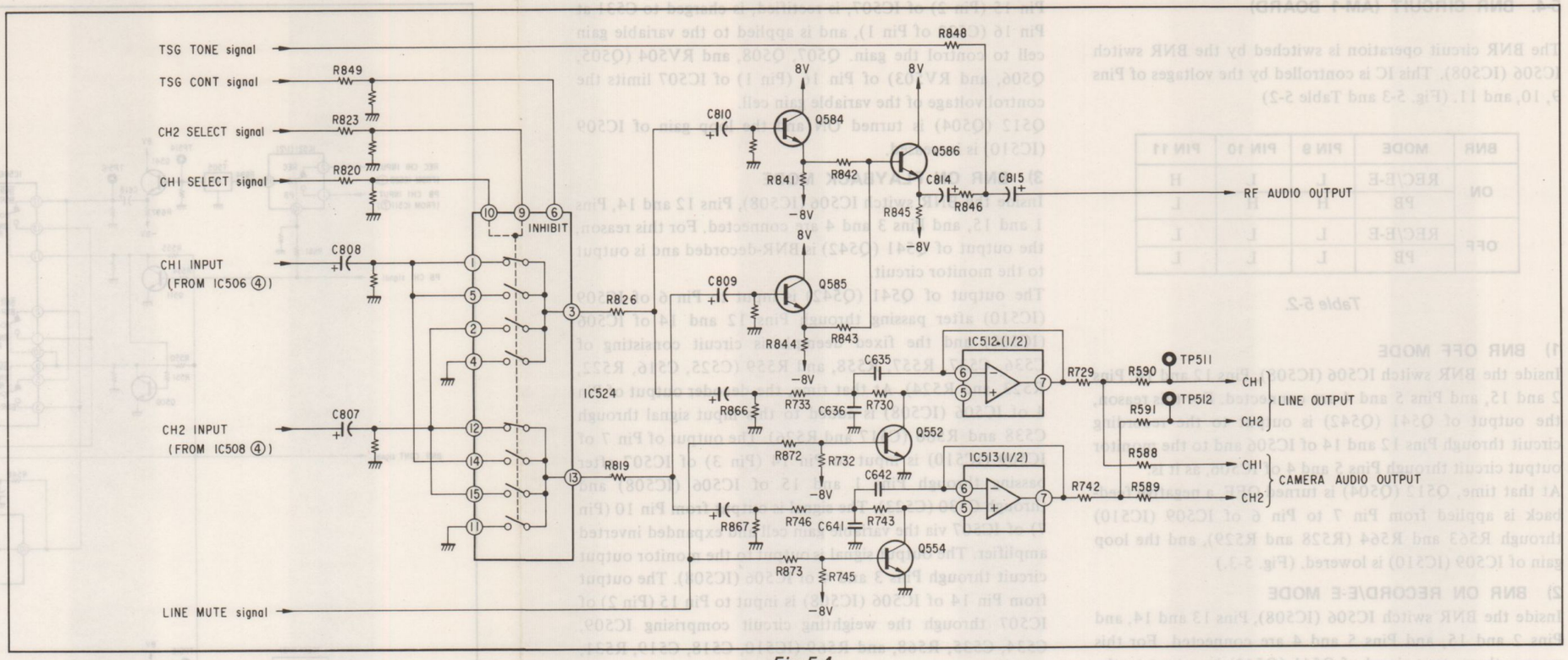


Fig. 5-4.

5-6. RECORD CIRCUIT (AM-1 BOARD)

The output signal of Pin 14 of the BNR switch IC506 (IC508) is input to Pin 3 of the RECORD AMP IC512 (IC513) through the REC LEVEL adjust RV506 (RV507). L501, R724, and C637 (L502, R737, and C644) are connected to Pins 1 and 2 of this IC to compensate high frequency characteristics. The output of Pin 1 of IC512 (IC513) is mixed with the REC bias current and is impressed to the REC head after passing through R721 and C631 (R734 and C638) and bias trap LV501 and C565 (LV502 and C564). Pin 3 of IC512 (IC513) is connected to Q511 (Q553). This transistor normally mutes CH1 (CH2) REC signals. However, muting is released during the REC or AUDIO DUB CH1 and CH2 (REC or AUDIO DUB CH1 and CH2, or AUDIO DUB CH2).

TP507 of CH2 connects the crosstalk cancel circuit (RV512, R603, R604, C578, and C579). In the AUDIO DUB CH2 mode, the REC state is set up for CH2, and PLAYBACK state, for CH1. For this reason, crosstalk generates from CH2 to CH1 in the audio head. To cancel the crosstalk, REC signals of CH2 are applied to the emitter of the first-stage transistor Q522 of CH1.

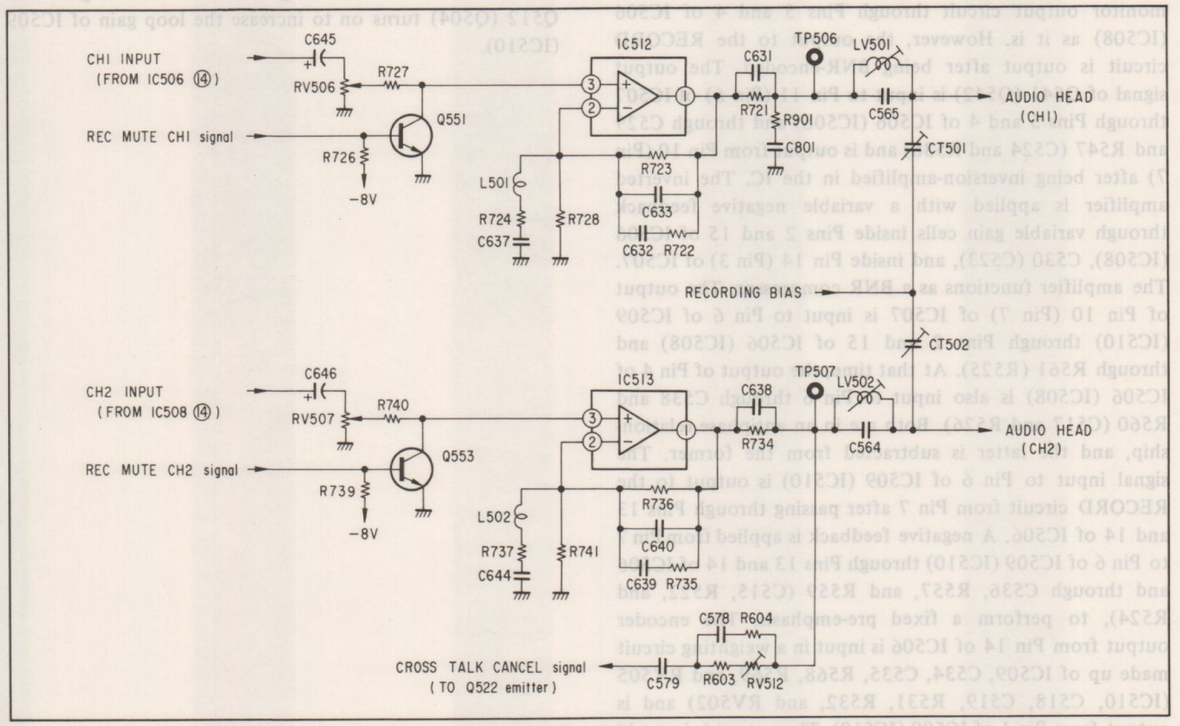


Fig. 5-5.

5-7. BIAS OSCILLATION CIRCUIT (AM-1 BOARD)

The bias circuit consists of Q513, T501, C568, C569, C570, R575, and R577. Q517, Q605, and Q616 control the bias oscillation. Q616 turns OFF and Q605 turns ON when the level of the BIAS CONT signal is H and that of the BRAKE OFF signal is L, turning ON Q517 and supplying 12V to the bias oscillation circuit, thus operating the oscillation circuit.

The REC bias current is applied from Pin 6 of T501 to the audio head through CT501 (CT502). The erase current is impressed from Pin 5 to the FULL ERASE HEAD, AUDIO CH1 ERASE HEAD, and AUDIO CH2 ERASE HEAD. First, during the REC mode, the level of the REC signal becomes H to operate RY503 and to shortcircuit LV503. The level of the DUB CH2 signal is L, and RY504 does not operate. For this reason, an erase current is flowed to all these three erase heads. Next, in the AUDIO DUB CH1 and CH2 mode, the level of the REC signal becomes L, shorting the FULL ERASE HEAD. Instead, an erase current flows to the dummy coil LV503. The level of the DUB CH2 signal is L, and an erase current flows to the other two erase heads as in the REC mode. Lastly, the level of the REC signal is L during the AUDIO DUB CH2 mode, as in the REC mode, and the FULL ERASE HEAD does not operate. The level of the DUB CH2 signal becomes H, and RY504 operates. An erase current is applied to the dummy coil L506, instead of to the AUDIO CH1 ERASE HEAD. As a result, only the AUDIO CH2 ERASE HEAD operates.

5-8. REC/PLAYBACK HEAD SELECTION CIRCUIT (AM-1 BOARD)

The level of the PB CH1 signal (PB CH2 signal) becomes H during the PLAYBACK or AUDIO DUB CH2 mode (PLAYBACK mode), operating RY501 (RY502). The audio head of CH1 (CH2) functions as a playback head. In all other instances, the head functions as a REC head.

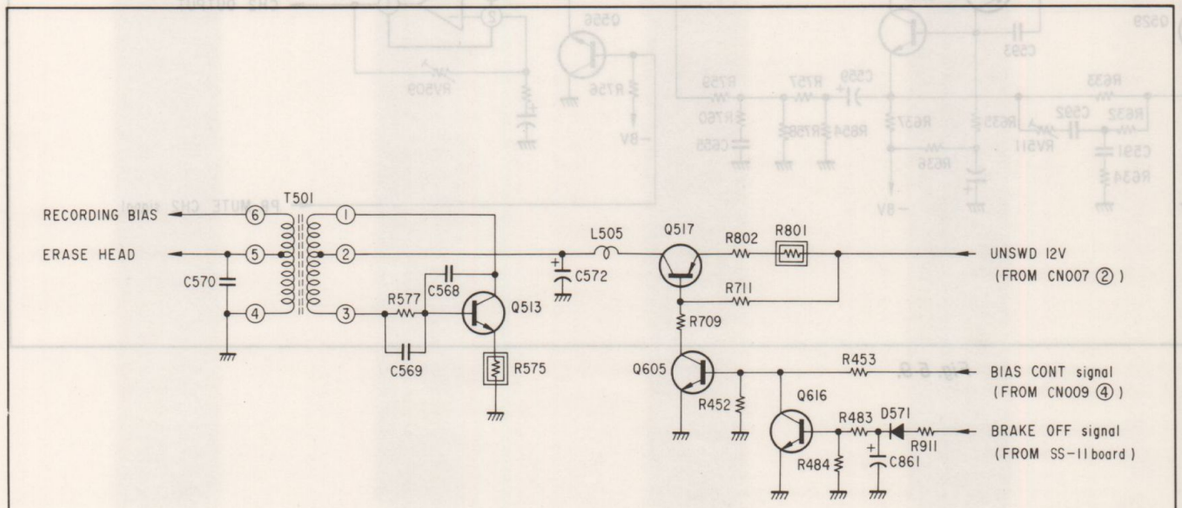


Fig. 5-6.

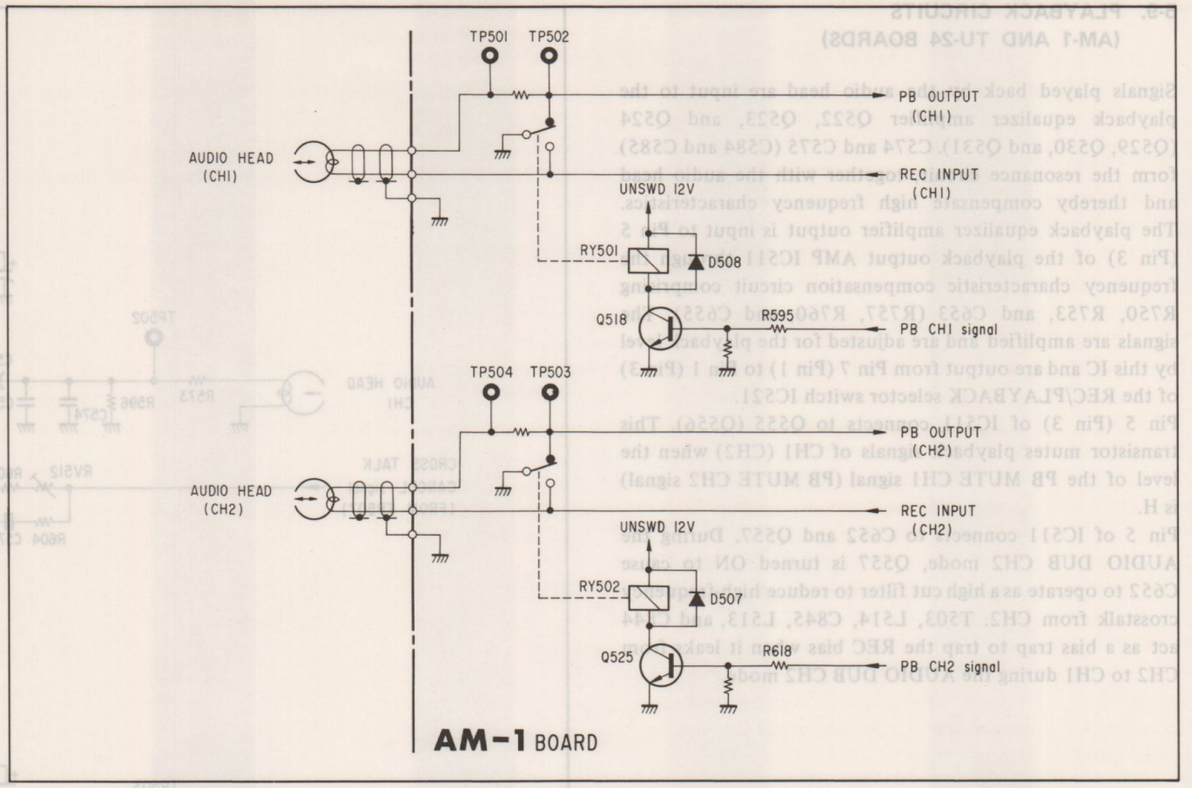


Fig. 5-7.

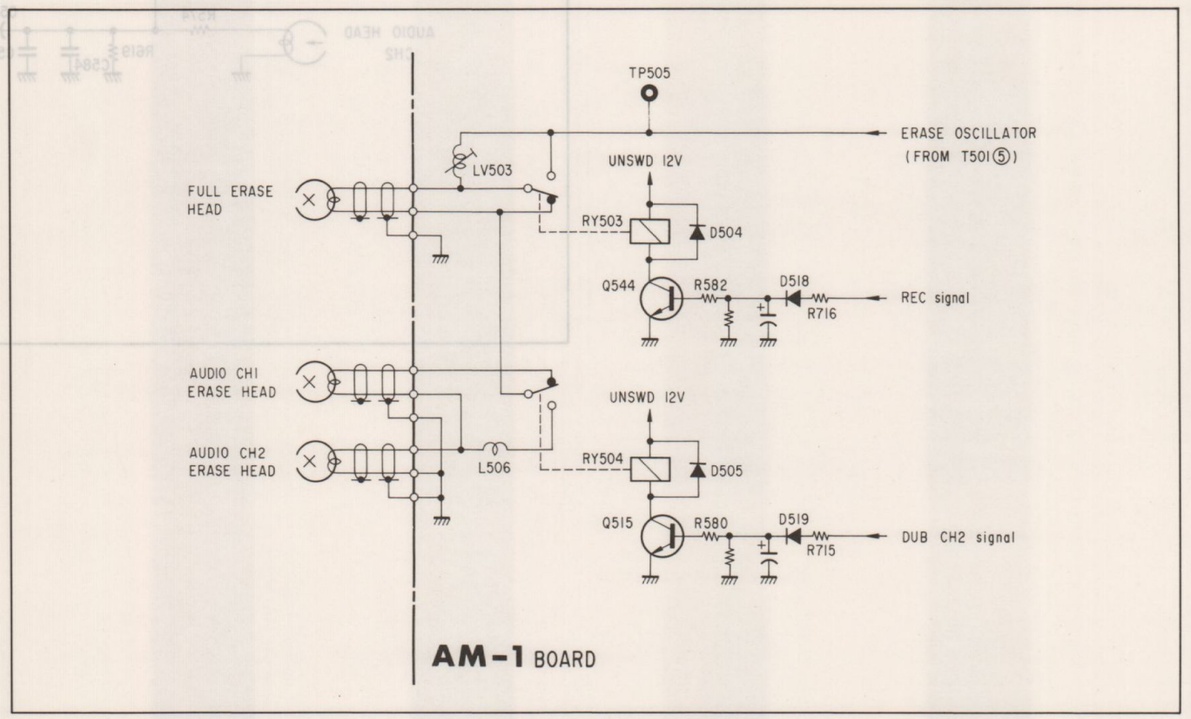


Fig. 5-8.

5-9. PLAYBACK CIRCUITS (AM-1 AND TU-24 BOARDS)

Signals played back by the audio head are input to the playback equalizer amplifier Q522, Q523, and Q524 (Q529, Q530, and Q531). C574 and C575 (C584 and C585) form the resonance circuit, together with the audio head and thereby compensate high frequency characteristics. The playback equalizer amplifier output is input to Pin 5 (Pin 3) of the playback output AMP IC511 through the frequency characteristic compensation circuit comprising R750, R753, and C653 (R757, R760, and C655). The signals are amplified and are adjusted for the playback level by this IC and are output from Pin 7 (Pin 1) to Pin 1 (Pin 3) of the REC/PLAYBACK selector switch IC521.

Pin 5 (Pin 3) of IC511 connects to Q555 (Q556). This transistor mutes playback signals of CH1 (CH2) when the level of the PB MUTE CH1 signal (PB MUTE CH2 signal) is H.

Pin 5 of IC511 connects to C652 and Q557. During the AUDIO DUB CH2 mode, Q557 is turned ON to cause C652 to operate as a high cut filter to reduce high-frequency crosstalk from CH2. T503, L514, C845, L513, and C844 act as a bias trap to trap the REC bias when it leaks from CH2 to CH1 during the AUDIO DUB CH2 mode.

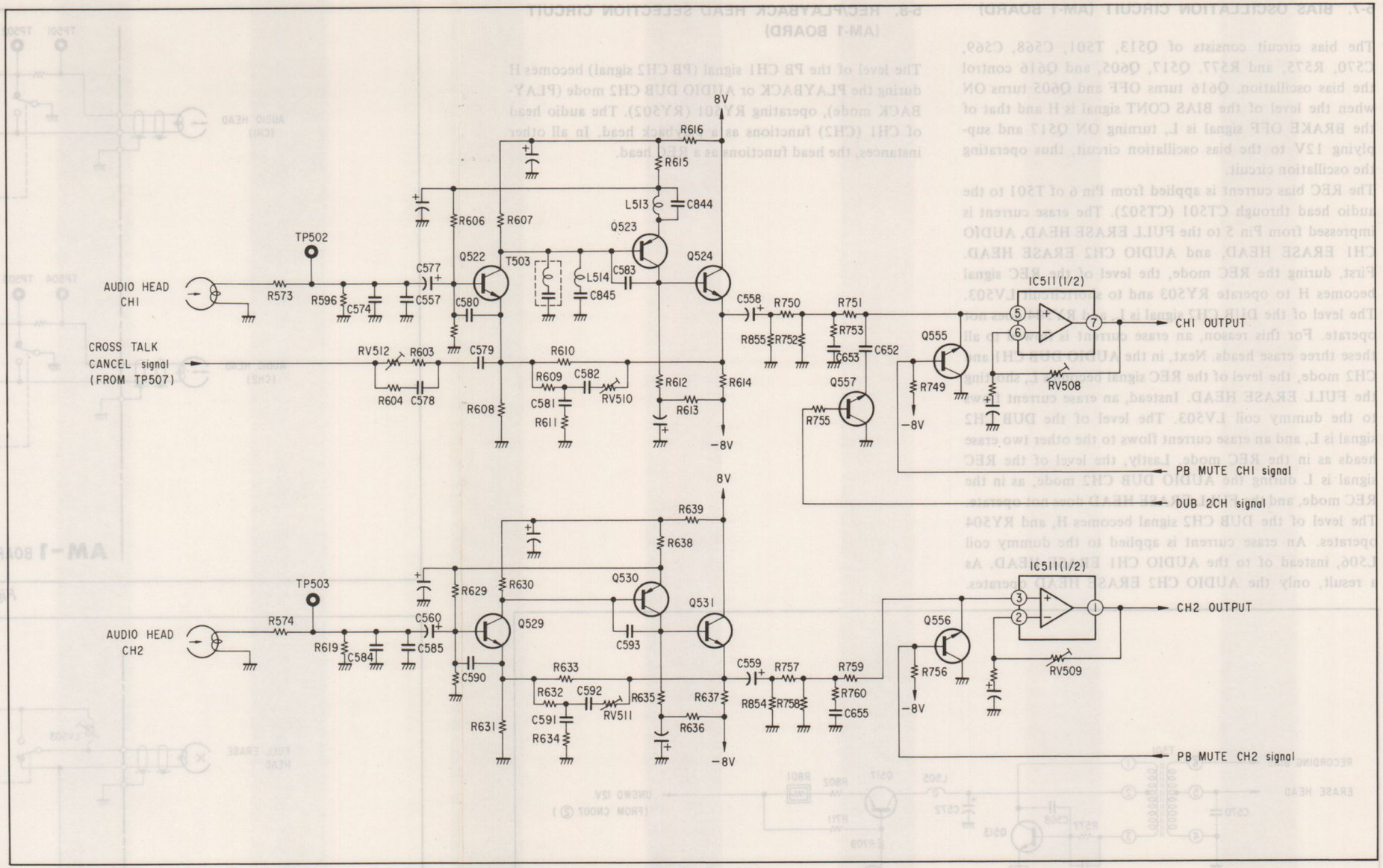


Fig. 5-9.

The CH2 playback output from Pin 1 of IC511 is sent to the stereo discrimination circuit on the TU-24 board. The circuit selects stereo discrimination signals of an extremely low level at 12.5 Hz overlapped on CH2 of recorded stereo tapes sold on the market, by means of the active band pass filter IC201. The discrimination signals are amplified by IC202 and are rectified in D201 and D202 to obtain a d.c. voltage. The voltage is input to Pin 3 of IC202 and is compared with the reference voltage of Pin 2 of IC202, lighting the stereo indicator where its level is higher.

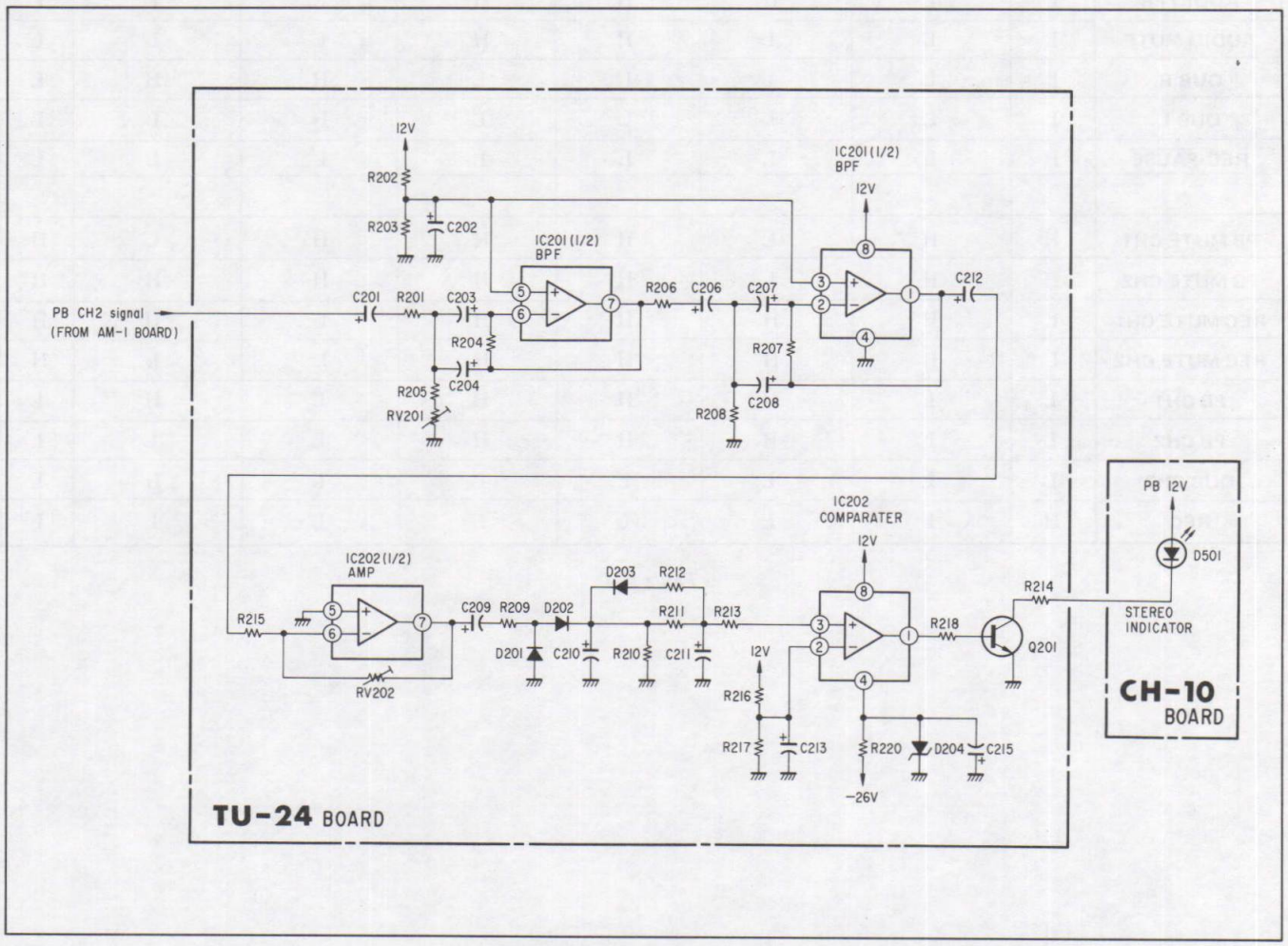


Fig. 5-10.

5-10. AUDIO SYSTEM CONTROL CIRCUIT

The circuit produces signals to control the audio circuits based on signals sent by the system control circuit on the SS-11 board.

MODE / SIGNAL	REC	REC·PAUSE	NORMAL PLAY BACK	PB·PAUSE	VARIABLE SPEED PLAYBACK	AUDIO DUB CH1, 2	AUDIO DUB CH2	E-E
BIAS CONT	H	L	L	L	L	H	H	L
AUDIO PB	L	L	H	H	H	L	L	L
AUDIO MUTE	L	L	L	H	H	L	L	L
DUB R	L	L	L	L	L	H	H	L
DUB L	L	L	L	L	L	H	L	L
REC·$\overline{\text{PAUSE}}$	H	L	L	L	L	L	L	L
PB MUTE CH1	H	H	L	H	H	H	L	H
PB MUTE CH2	H	H	L	H	H	H	H	H
REC MUTE CH1	L	H	H	H	H	L	H	H
REC MUTE CH2	L	H	H	H	H	L	L	H
PB CH1	L	L	H	H	H	L	H	L
PB CH2	L	L	H	H	H	L	L	L
DUB CH2	L	L	L	L	L	L	H	L
REC	H	L	L	L	L	L	L	L

Table 5-4.

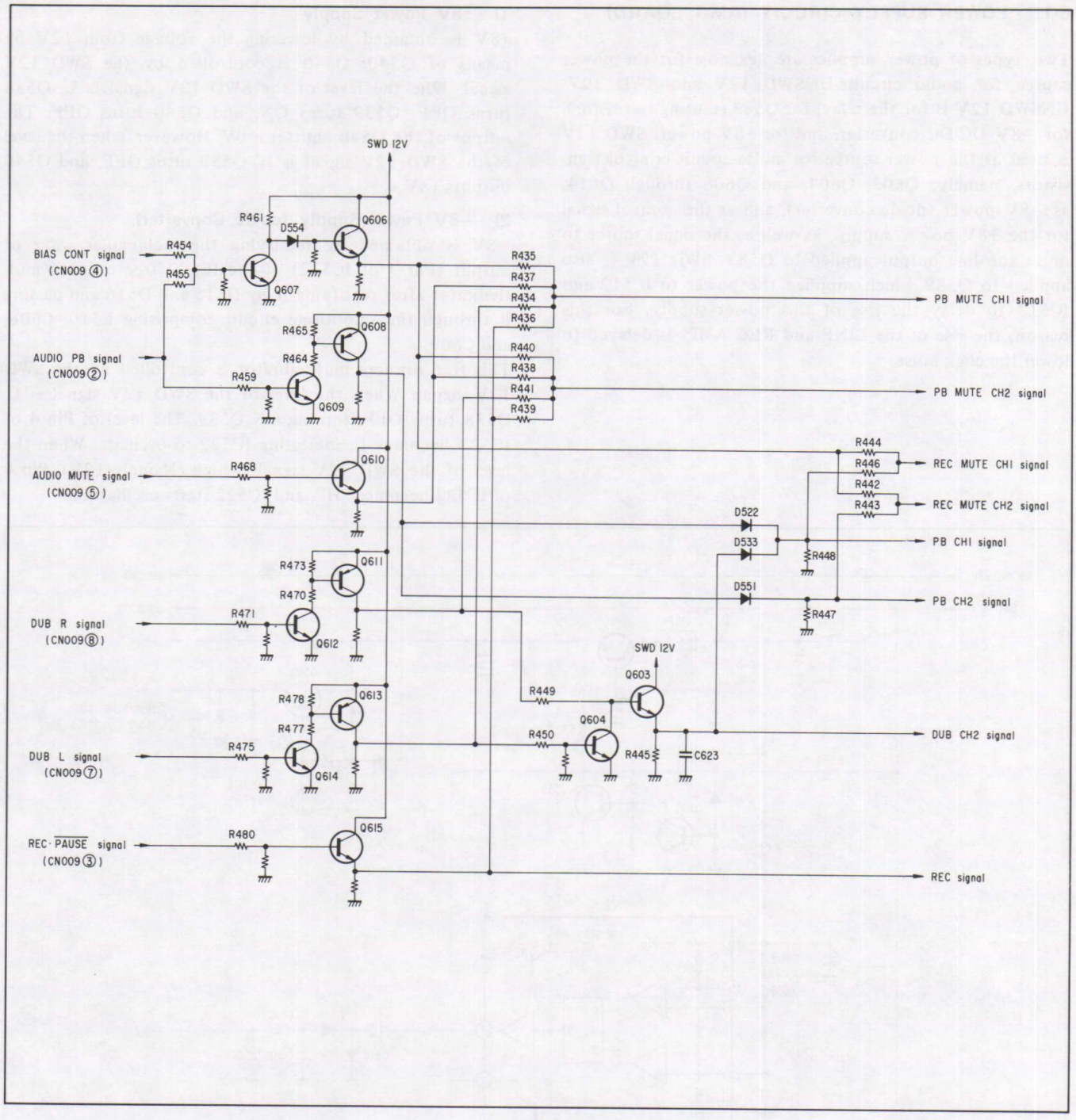


Fig. 5-11.

5-11. POWER SUPPLY CIRCUIT (AM-1 BOARD)

Two types of power supplies are available for the power source for audio circuits-UNSWD 12V and SWD 12V. UNSWD 12V is for the relay, for Q583 (muting transistor), for −8V DC-DC converter, and for +8V power. SWD 12V is used as the power source for audio-circuit control transistors, namely, Q603, Q604, and Q606 through Q614, as −8V power (dc-dc converter), and as the control signal for the +8V power supply, as well as the signal source to mute the line output applied to Q583. SWD 12V is also applied to Q589 which supplied the power to IC512 and IC513 to delay the rise of this power supply. For this reason, the rise of the LINE and REC AMPs is delayed to lower the click noise.

1) +8V Power Supply

+8V is obtained by lowering the voltage from 12V by means of Q540. Q540 is controlled by the SWD 12V signal. Whe the level of the SWD 12V signal is L, Q538 turns OFF, Q539 turns ON, and Q540 turns OFF. The output of the Q540 emitter is 0V. However, when the level of the SWD 12V signal is H, Q539 turns OFF, and Q540 outputs +8V.

2) −8V Power Supply (dc-dc Converter)

−8V is obtained by rectifying the rectangular wave of output (Pin 3 of IC522) of the IC522 free running multivibrator after rectifying it by D515 and D516 and passing it through the smoothing circuit comprising L510, C608, and C609.

This free running multivibrator is controlled by the SWD 12V signal. When the level of the SWD 12V signal is L, Q538 turns OFF, turning ON Q539. The level of Pin 4 of IC522 becomes L, inhibiting IC522 to oscillate. When the level of the SWD 12V signal is high (Namely 12V), Pin 4 of IC522 becomes "H", and IC522 starts oscillating.

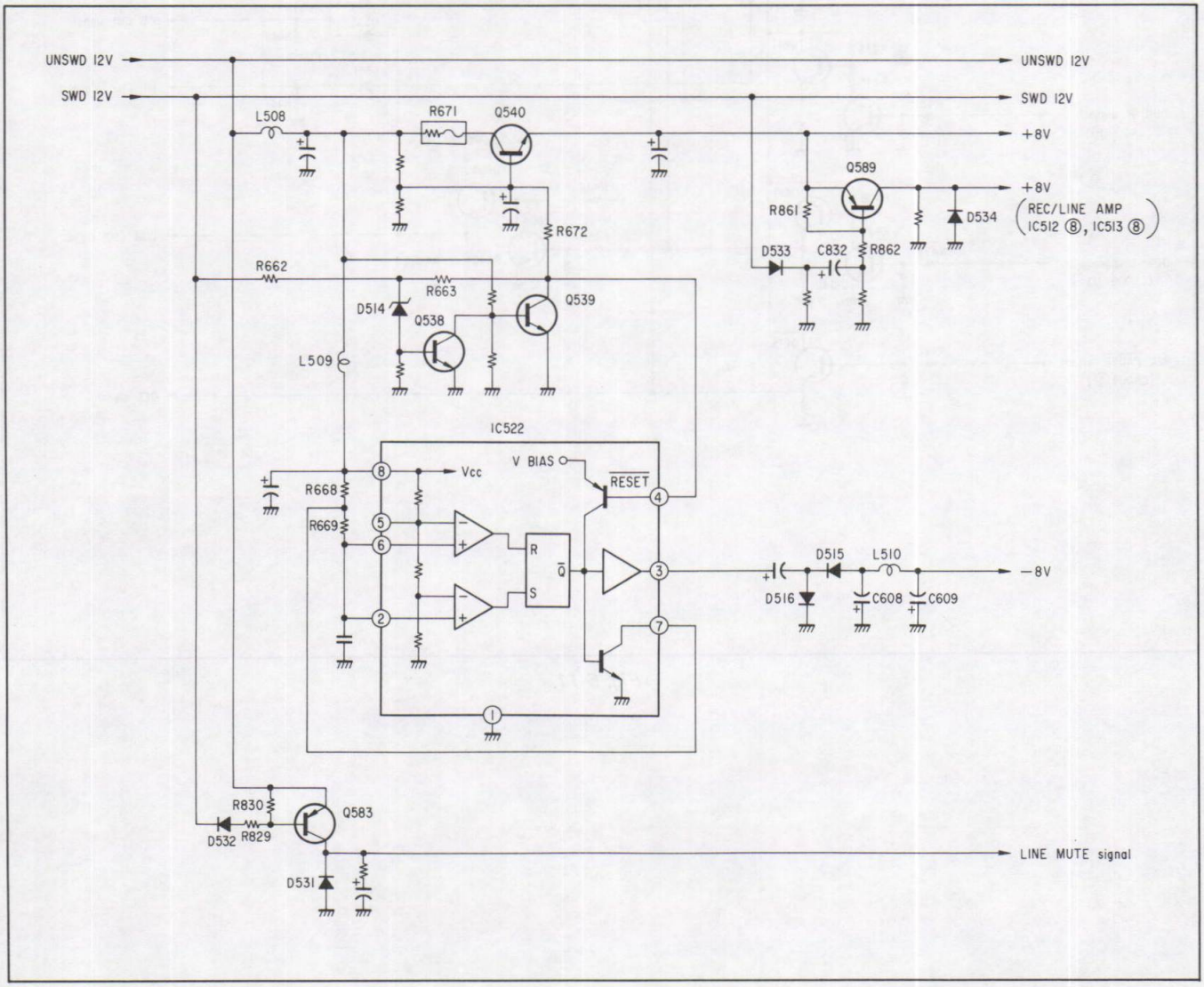


Fig. 5-12.

SECTION 6
TIMER CIRCUIT

6-1. FUNCTION

- Quartz oscillator
- 24-hour display
- Week and data display
- Automatic program searcher (APS) display
- Program (channel) display
- 2-week/9-event (program)
  (over 2 weeks, 9 programs are possible)
- Counter display
- Recording by timer:
  TURN ON TIME, TURN OFF TIME
  EVERY DAY: When the turn on time and turn off time are set on the timer without specifying a day of the week, recording can be made daily at the set time.
  EVERY WEEK: By using "EVENT 9" only, weekly picture recording can be programed by the timer on a specified day of the week.

6-2. MB88401 OPERATION

PIN FUNCTIONS

Pin No.	Designation	Meaning	I/O	Function and Operation
1	R_4	GR_0	O	Display 2G
2	R_5	GR_1	O	Display 3G
3	R_6	GR_2	O	Display 4G
4	R_7	GR_3	O	Display 5G
5	R_8	GR_4	O	Display 6G
6	R_9	GR_5	O	Display 7 G
7	R_{10}	GR_6	O	Display 1G, 8G
8	R_{11}	GR_7	O	Display 9G
9	R_{12}	SD	O	Prog. No. display flashing signal
10	R_{13}	PWR	O	Power switch toggle output
11	R_{14}	K PORT EXTENSION	O	Imput port timing signal
12	K_0		I	Matrix input from key scan & extension ports
13	K_1		I	
14	K_2		I	
15	K_3	K_3	I	
16	Ex	Ex	I	Quarts for time base
17	X	X	O	
18	RST	RESET	I	Power on reset
19	IRQ	CTR RESET	I	Counter reset
20	TC	TC		
21	Vss			GND
22	SC/TO	CTR PLS	I	Counter pulse
23	SI	CTR UP	I	Counter up
24	SO		O	
25	O_0	PR LOCK	O	Channel select inhibit signal
26	O_1	DO_0	O	a segment display lighting signal
27	O_2	DO_1	O	b segment display lighting signal
28	O_3	DO_2	O	c segment display lighting signal

Table 6-1. (1/2)

Pin No.	Designation	Meaning	I/O	Function and Operation
29	O_4	DO_3	O	d segment display lighting signal
30	O_5	DO_4	O	e sigment display lighting signal
31	O_6	DO_5	O	f sigment display lighting signal
32	O_7	DO_6	O	g segment display lighting signal
33	P_0	DP_0	O	P_1 segment display lighting signal & timer switch matrix
34	P_1	DP_1	O	P_2 segment display lighting signal & timer switch matrix
35	P_2	DP_2	O	P_3 segment display lighting signal & input port timing signal
36	P_3	DP_3	O	P_4 segment display lighting signal & input port timing signal
37	R_0	PR UP	O	Program up signal
38	R_1	PR RST	O	Program reset signal
39	R_2	CTR DISP	O	Counter display signal output to system control circuit
40	R_3	TIMER REC	O	Timer REC signal output to system control circuit
41		V_M		Power source for memory. Connected to V_{DD}
42				5V Power source

Table 6-2. (2/2)

6-3. INPUT MATRIX

I \ O	P_3	P_2	P_1	P_0	O_7
K_0	APS A	POWER ON OFF	CLEAR KEY	COUNTER/TIMER	FAST (MINUTE)
K_1	APS B	REC READY	NEXT STEP KEY	CLOCK SET KEY	FAST (HOUR)
K_2	APS C	PWR FAILURE	SELECT + KEY	TIMER SET KEY	
K_3	APS D	12/30 CH	SELECT – KEY	TIMER REC KEY	REC PAUSE

Table 6-2.

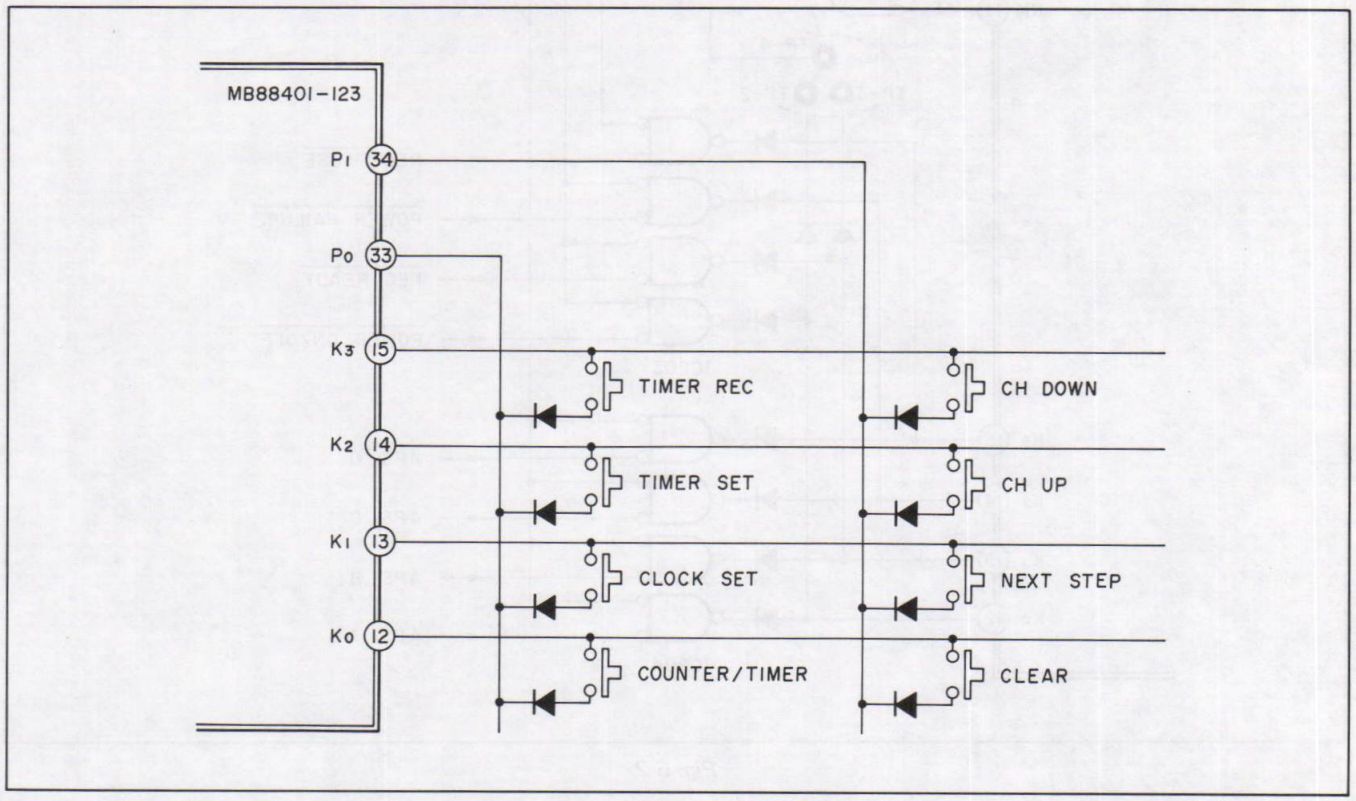


Fig. 6-1.

Keyed-in data is read by the microcomputer every 10ms, but effective only when input is continuous for more than three input cycles. This is to prevent erroneous operation due to chattering.

That is, the keys must be depressed for 30ms or longer to be recognized.

(1) EXTENSION PORTS

Since the microcomputer does not have a sufficient number of input ports, input signals are time-shared by external and internal time-sharing pulses.

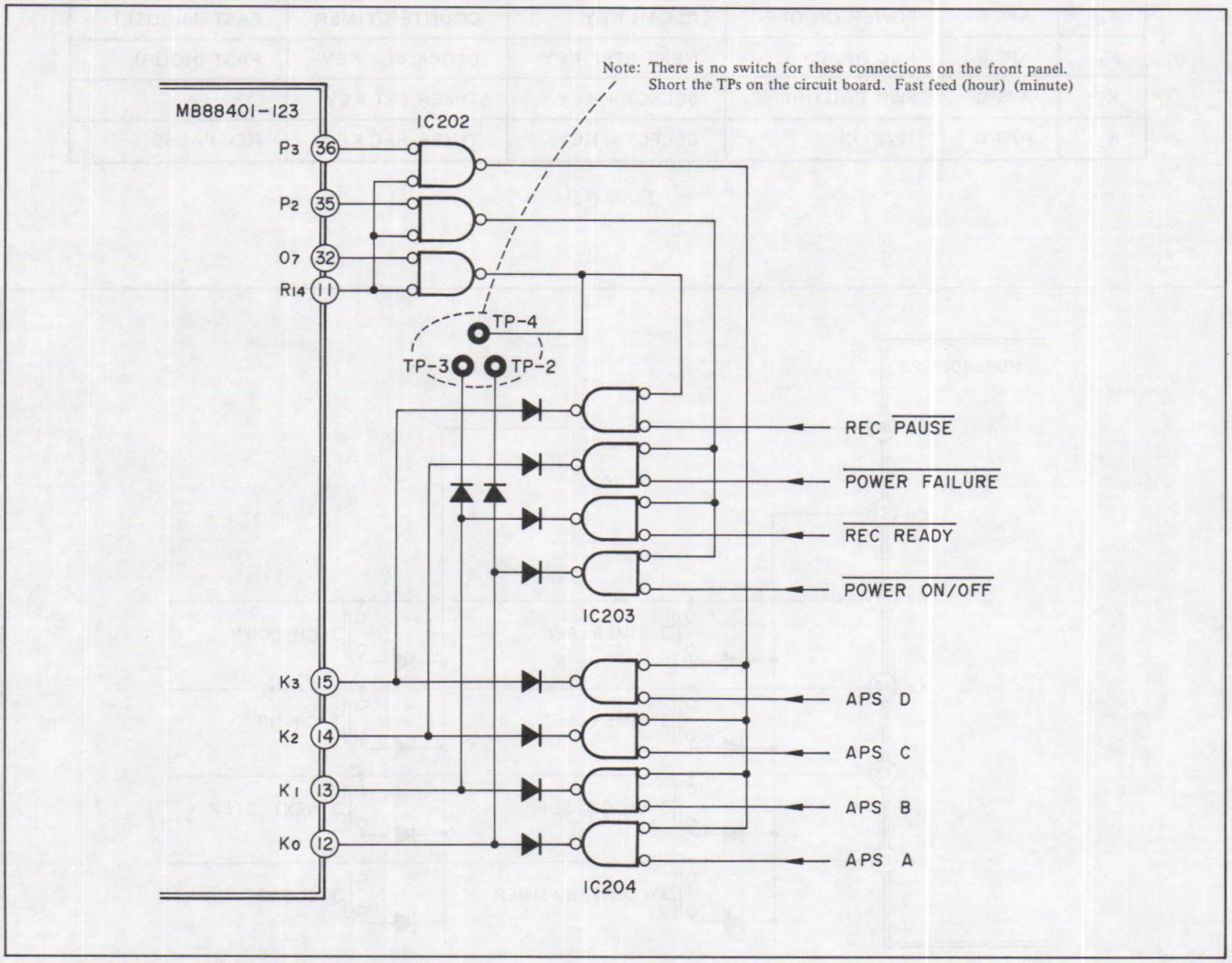


Fig. 6-2.

(2) FAST FEED

Shorting TP4 and TP3 will advance the hour display at 0.1 second intervals (360.000 times faster than normal), and shorting TP4 and TP2 will advance the minute display at 0.1 second intervals (600 times faster than normal).

6-4. TIMER OPERATION

The timer is operated in the main by a 4K byte N-MOS 4-bit microcomputer IC201, and its setting is achieved by keys S301 through S307, respectively named CLOCK SET, TIMER SET, CLEAR, DOWN, UP, NEXT STEP, and TIMER REC.

The key actuation signals are output from P1 and P2 of IC201, and are input through K0 through K3 by a diode matrix.

The POWER ON/STANDBY states of the set are controlled by timers. With the ON/STANDBY key depressed, the timers control the ON-OFF switching and, for the shift from POWER OFF to TIMER SET MODE, and from TIMER REC STANDBY to MONITOR and TIMER REC, switching from STANDBY to ON, and from ON to STANDBY.

(1) INPUT SELECTOR DISPLAY

Program Nos. are displayed by the hardware. When the input selector is set to LINE/PCM, "AU" (AUXILIARY) is displayed. When it is set to TUNER, "PROG" and the selected program Nos. are displayed, and when it is set to CAMERA, "CA" is displayed.

The input selector display is static drive using on exclusive drive circuit. Other displays are dynamic drive.

(2) APS DISPLAY

Binary codes (positive logic) from the system control are input through extension ports, decoded in the microcomputer, and transmitted to the driver for display.

(3) COUNTER DISPLAY

For the COUNTER display, the COUNTER/TIMER key is toggled between the TIMER display and COUNTER display with POWER ON. The maximum display is ±9H59M59S.

It is a 1 count/second linear counter, driven by pulses obtained by 1/25 frequency division of the CTL from the system control.

(4) REC $\overline{\text{PAUSE}}$ signal

When the timer is set during recording, the channel changes which is undesirable. To avoid this, the REC $\overline{\text{PAUSE}}$ signal is taken in to prevent the system from entering the TIMER SET mode even when the TIMER SET key is pushed, and the TIMER SET mode is cleared when the REC $\overline{\text{PAUSE}}$ becomes high in the TIMER SET mode.

i) Channel set timing
(When selecting channel N)

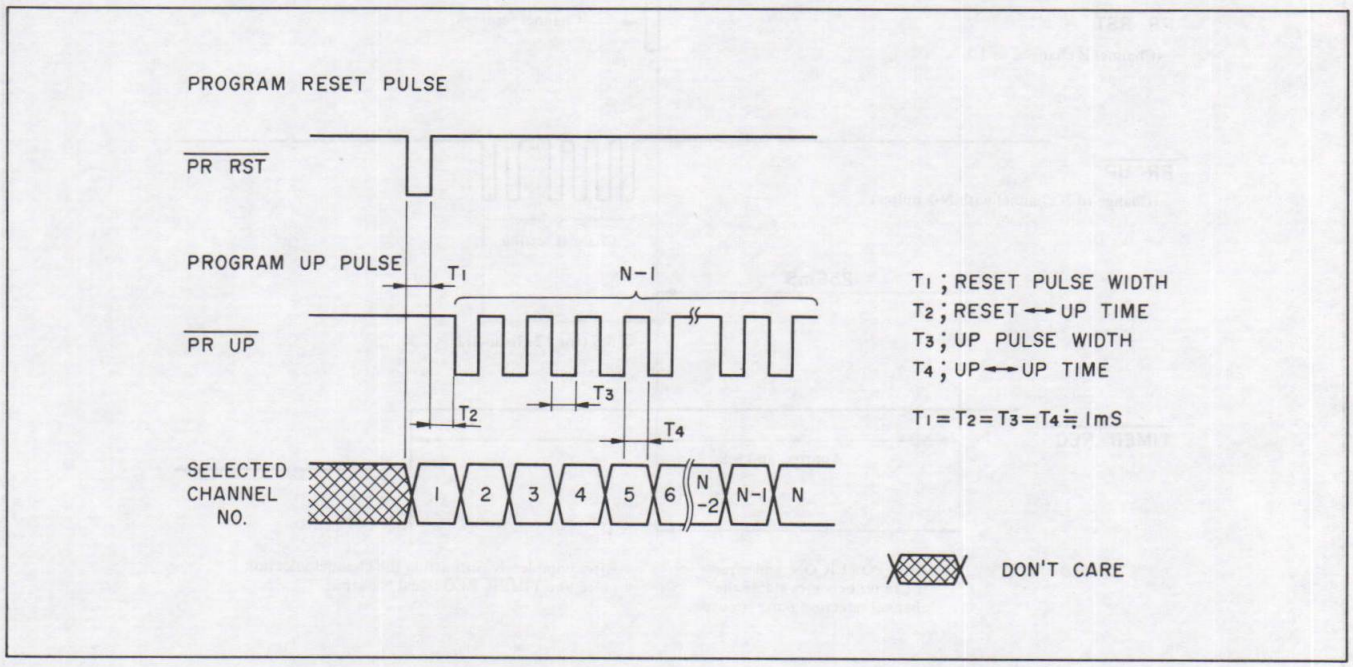


Fig. 6-3.

When RESET, the tuner channel becomes 1.
Then, the channel numbers are increased by UP PULSEs.

Example: To select channel 5, output one reset pulse, and then, output four up pulses.

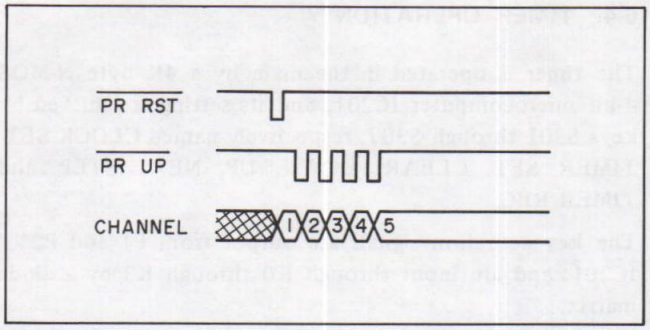
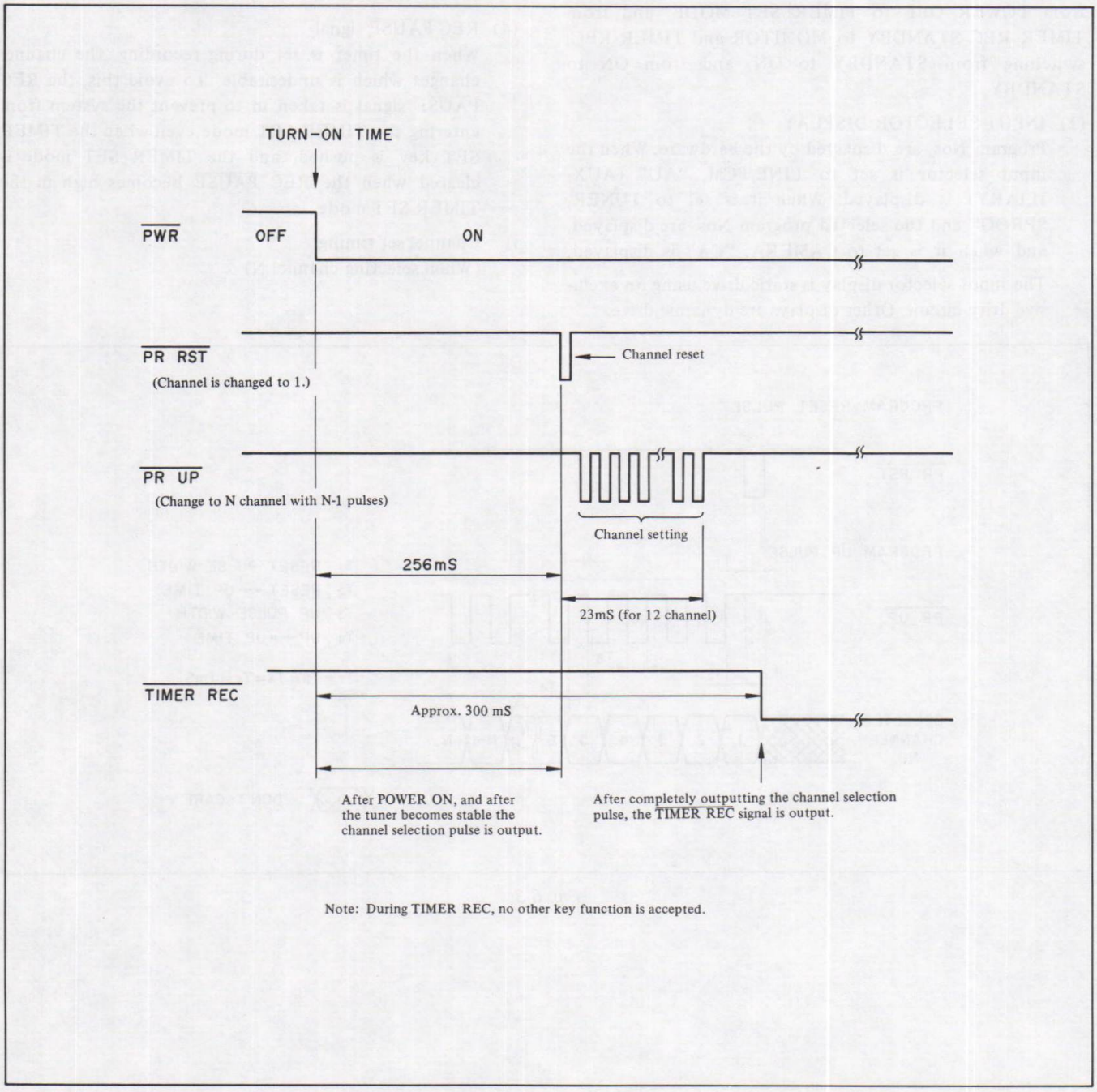


Fig. 6-4.

ii) Timer REC timing



Note: During TIMER REC, no other key function is accepted.

Fig. 6-5.

6-5. SUB POWER CONTROL

The control path for the sub power supply is as shown below.
The sub power supply is turned on and off in the following three modes.

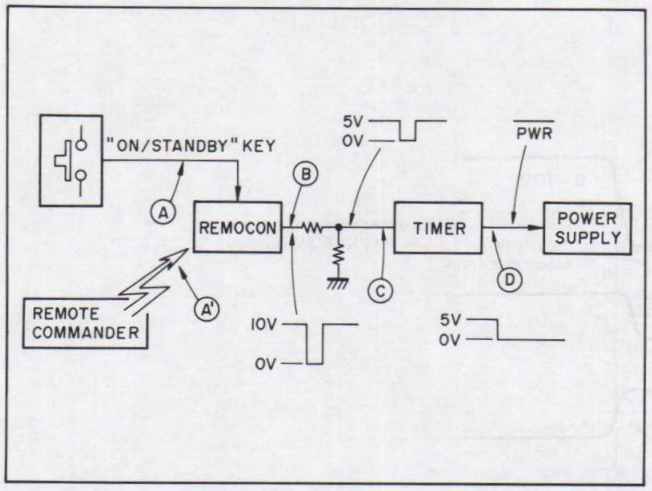


Fig. 6-6.

(1) When the ON/STANDBY key is pushed while in the manual mode.

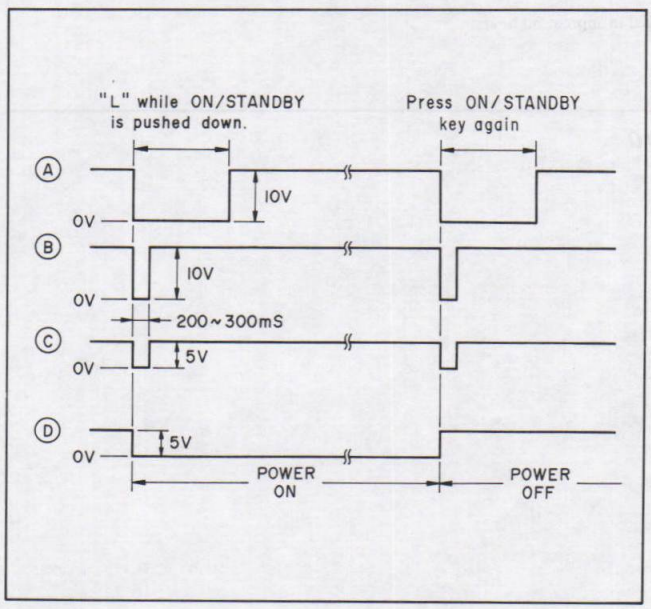


Fig. 6-7.

(2) When the ON button is pushed on the remote commander.

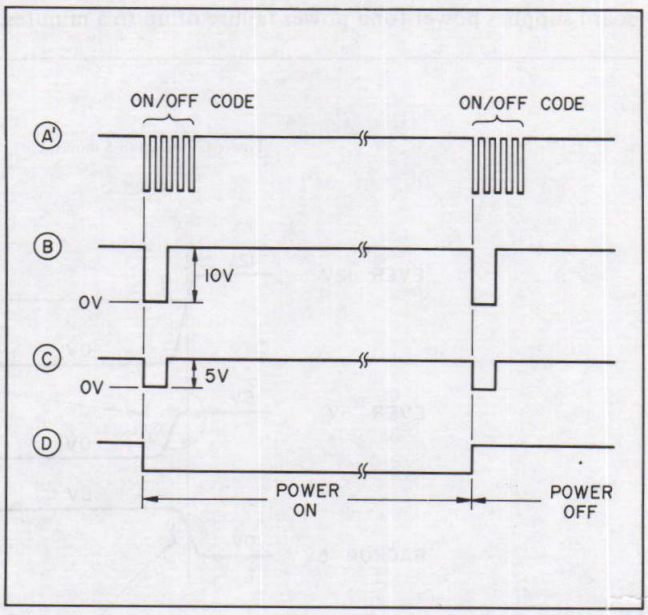


Fig. 6-8.

(3) When reserve setting, reserve checking and reserve execution with the timer.

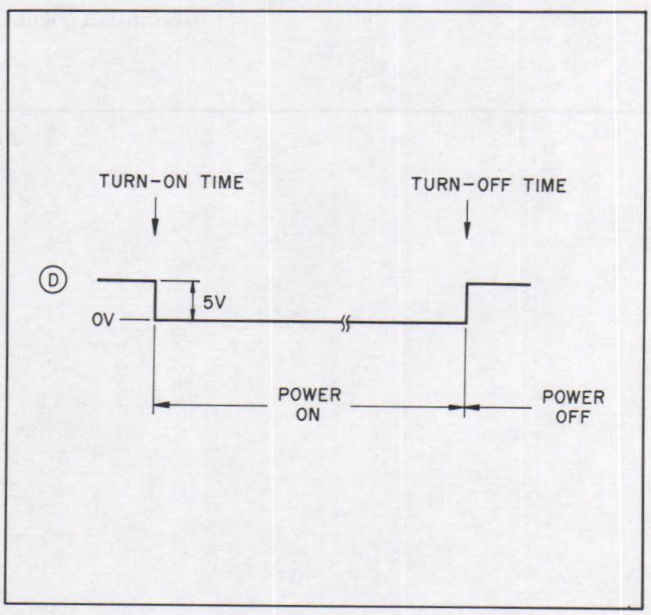
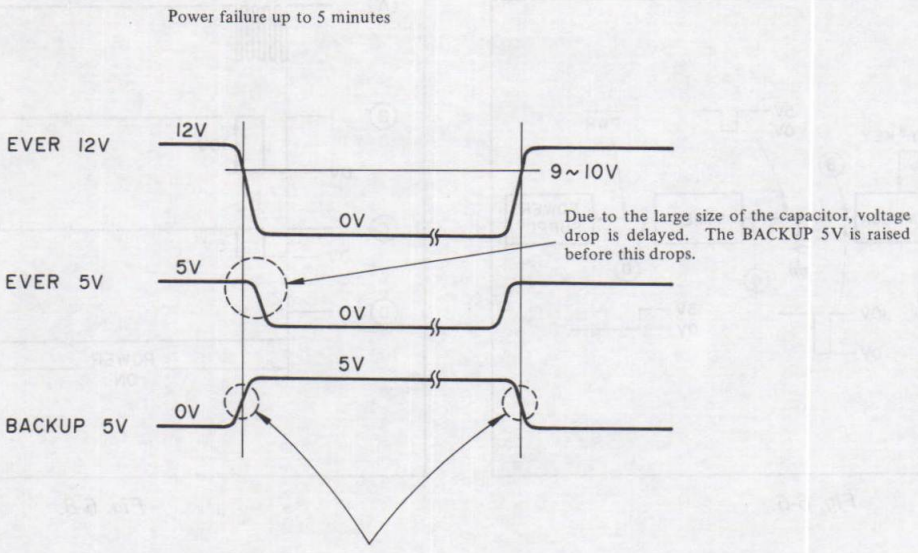


Fig. 6-9.

6-6. POWER FAILURE BACKUP

The battery backup circuit incorporated in the TU-24 board supplies power for a power failure of up to 5 minutes.



When EVER 12V drops to 9 ~ 10V, the backup circuit starts to oscillate to generate BACKUP 5V.
When EVER 12V rises above 9 ~ 10V, oscillation stops, and charging begins.

Note: The backup battery is charged in approx. 30 hours.

Fig. 6-10.

SECTION 7
TUNER/IF CIRCUIT

7-1. VOLTAGE SYNTHESIZER CONTROLLER M50118P

General

The basic operation is the same as that of the SL-C7E system. Both M50118P and M5G1400P are used as a controller and memory respectively in this system.

1) Automatic Programming (AP)

When the AP SW (Automatic Programming switch) has been pressed, the prog. No. and VC voltage are set to "1" and band I "low end" automatically, and "search up" is started.

When a broadcast has been received, "search up" stops, and tuning data (VC voltage, prog. No. and band data) are stored in the memory IC.

Thereafter, the prog. No. is increased by 1 automatically, and "search up" is started again.

If band data has been set to band U "high end" or where the prog. No. has been set to "0", AP stops automatically. Prog. No. is set to "1" and the broadcast stored in the memory, is received resulting in terminating the "search up" operation.

2) Manual Search

When the SEARCH + or – has been pressed instead of the AP SW, the present selected prog. No. does not change. "Search up or down" is started at the frequency.

When a broadcast has been received, "search" stops, and the tuning data is stored in the memory. Then the "search" procedure ends.

If the SEARCH SW has been pressed again, "search up or down" procedures start again.

When "search" mode is being executed, the search display LED and the front FLO "prog. No." are blinking.

The broadcast stored in the memory as a result of "search" mode is automatically set in a state of AFT ON.

3) Fine Tuning

When the FINE + or – SW has been pressed, AFT is turned off. If the switch is kept pressed, the tuning voltage goes up or down gradually. Even if the switch is released, the AFT remains OFF.

4) AFT

Pressing the AFT SW turns on the AFT (AFT OFF→AFT ON only). The AFT "LED" lights up during the time the AFT is switched ON.

5) RESET

When the RESET switch has been pressed after selecting a specified prog. No. to be reset, the tuning data is set as follows:

VC voltage = MIN, Band = Band I, AFT = OFF

6) Channel Selection/Remote Control Channel Selection

A channel can be selected using the prog. select SW or by means of remote control. The method used is the same in either case. When prog. No. 1 ~ 9 or 0 is to be selected, press the corresponding 1 ~ 9 or 0 switch. When prog. No. 10 ~ 19, or 20 ~ 29 are to be selected, press the 10 or 20 shift switch first. The tens digit prog. No. display is blinking until the units digit prog. No. switch is pressed. Where this switch is not subsequently pressed, this results in returning to the former prog. No. after approx. 6.5sec blinking.

7) Display

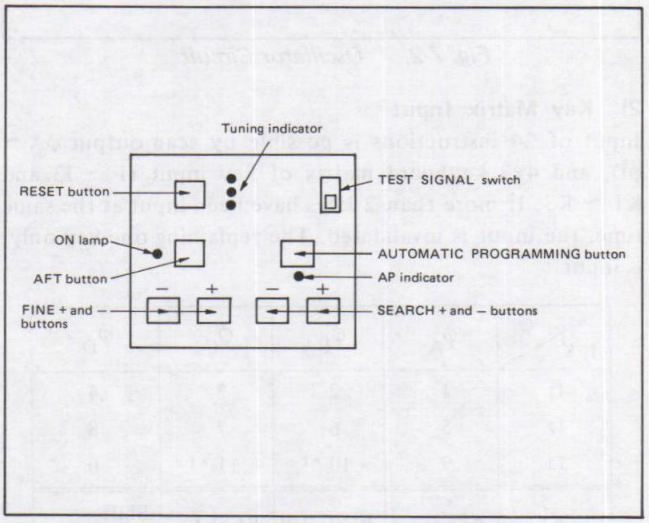


Fig. 7-1. Tuning Compartment

7-1-1. M50118P Operation Description

1) Oscillator

Since CMOS invertor and MOS resistance for feed back are provided in the IC, the oscillator can be composed of a ceramic resonator and two condensers. Oscillation frequency is 1.8 MHz.

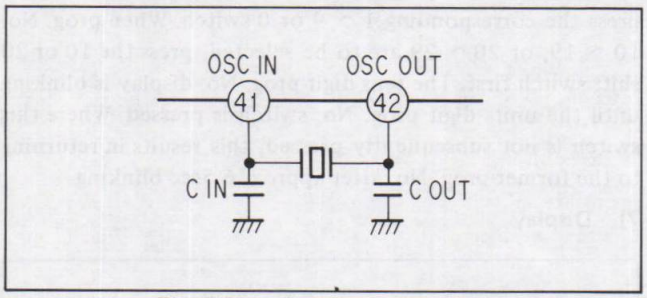


Fig. 7-2. Oscillator Circuit

2) Key Matrix Input

Input of 24 instructions is possible by scan output $\phi A \sim \phi D$, and 4x3 keyboard matrix of key input I1 ~ I3 and K1 ~ K3. If more than 2 keys have been input at the same time, the input is invalidated. The remaining one key only, is input.

I, K \ ϕ	ϕ_A	ϕ_B	ϕ_C	ϕ_D
I1	1	2	3	4
I2	5	6	7	8
I3	9	10 *1	11 *1	0
K1	AP	FINE UP	RESET	Shift 10
K2	S UP	FINE DN	AFT	Shift 20
K3	S DN	PR UP	PR DN	PR LOCK *2

*1 Unused on SL-C9E.
*2 Internal switch turned on/off by timer.

Table 7-1. Key matrix

3) $\overline{\text{PBEX}}$ Input

By input of the scan output $\phi A \sim \phi D$ for $\overline{\text{PBEX}}$ input, prog. No. and band can be changed-over.

Prog. \ ϕ	ϕ_A	ϕ_B	
30			SL-C9E
20	○		
12		○	SL-C9UB
10	○	○	

Table 7-2.

Band \ ϕ	ϕ_C	ϕ_D	
3			SL-C9E
4	○		
1 (U)		○	SL-C9UB

Table 7-3.

Note: "o" means "input".

4) Search

Automatic programming (AP) and manual search are available for search mode.
For the operation, refer to item 7-1 as mentioned before. In the case of channel selection during search, the search mode is released, and a channel is selected.

i) Search speed

Search speed at no signal is as follows;

Band	Sweep Time (sec.)
I	2.33
III	4.66
III', U	9.32

Table 7-4.

In the case of the following, the search speed is reduced to 1/16 of that at the non signal time.

(a) When AP, S UP;
Until "DN" input becomes "H" after "TB" input and "$\overline{\text{UP}}$" input are set to "H" and "L" respectively.

(b) When S DN;
Until "$\overline{\text{UP}}$" input becomes "L" after "TB" input and "DN" input are set to "H".

ii) Change-over of band during search mode

The band is changed-over as follows at the band high end or low end during search mode.

Number of Bands	Band Switching Sequence	
3	I ⟷ III ⟷ U	SL-C9E
4	I ⟷ III ⟷ III' ⟷ U	
1 (U)	U	SL-C9UB

Table 7-5.

iii) Prog. No. change-over during AP

Prog. No. is changed-over as follows when automatic programming (AP) is being executed.

Number of Programs	Program Number Switching Sequence	
10	Prog. 1→10	
12	Prog. 1→12	SL-C9UB
20	Prog. 1→19→0	
30	Prog. 1→29→0	SL-C9E

Table 7-6.

iv) Search Mode Display

When search is being executed, the search display "LED" blinks in an approx. 0.3sec cycle, at 50% duty.

5) Channel Selection

i) Key input

For channel selection by key input, refer to item 7-1(6) mentioned before.

ii) Channel selection by remote control timer

Direct channel selection or sequential channel selection is possible using the $\overline{\text{PR RST}}$, $\overline{\text{PR UP}}$ or $\overline{\text{PR DN}}$ terminals. The SL-C9E employs direct channel selection only.

(a) Direct channel selection

- Program 1 selection

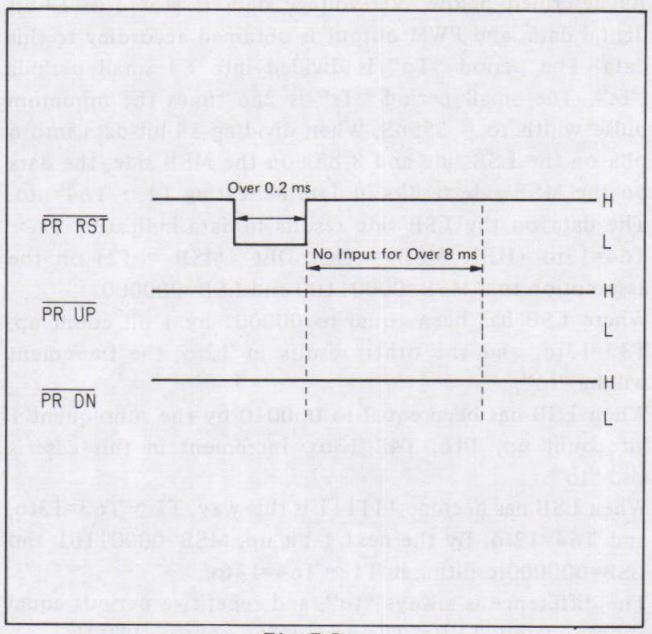


Fig. 7-3.

- Program 4 selection

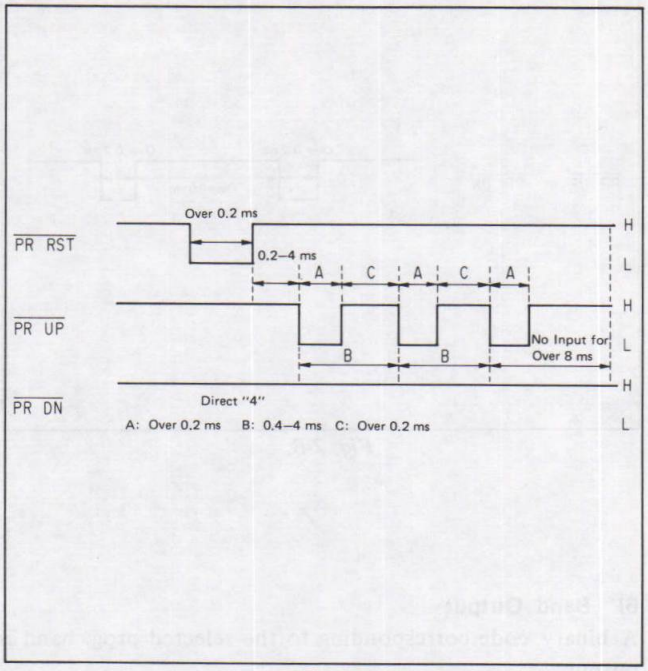


Fig. 7-4.

- Program 0 selection

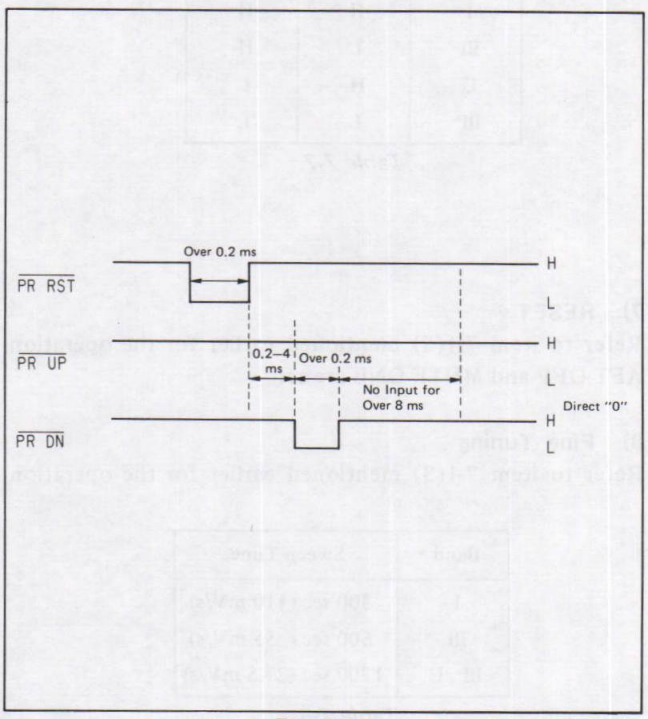


Fig. 7-5.

(b) Sequential channel selection

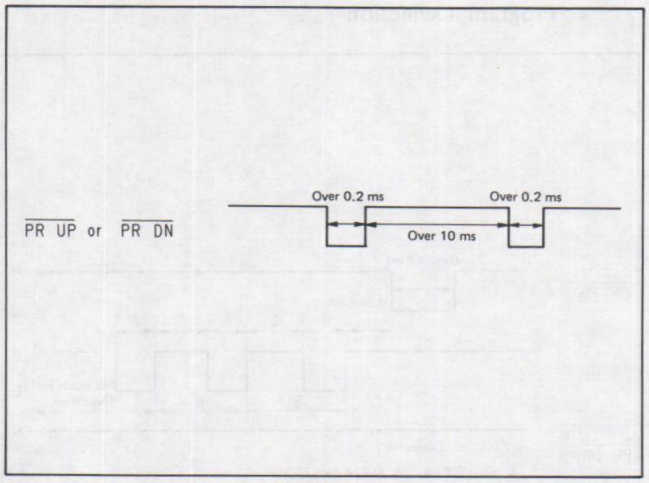


Fig. 7-6.

6) Band Output

A binary code corresponding to the selected prog. band is output.

Band	B1	B2
I	H	H
III	L	H
U	H	L
III'	L	L

Table 7-7.

7) RESET

Refer to item 7-1(5) mentioned earlier for the operation. AFT OFF and MUTE ONE are set.

8) Fine Tuning

Refer to item 7-1(3) mentioned earlier for the operation.

Band	Sweep Time
I	300 sec (110 mV/s)
III	600 sec (55 mV/s)
III', U	1200 sec (27.5 mV/s)

Table 7-8.

9) AFT SW

Refer to item 7-1(4) mentioned earlier for the operation.

10) Search Stop Circuit

Search is controlled by input of UP, DN or TB. The TB shows YES/NO of a video signal.

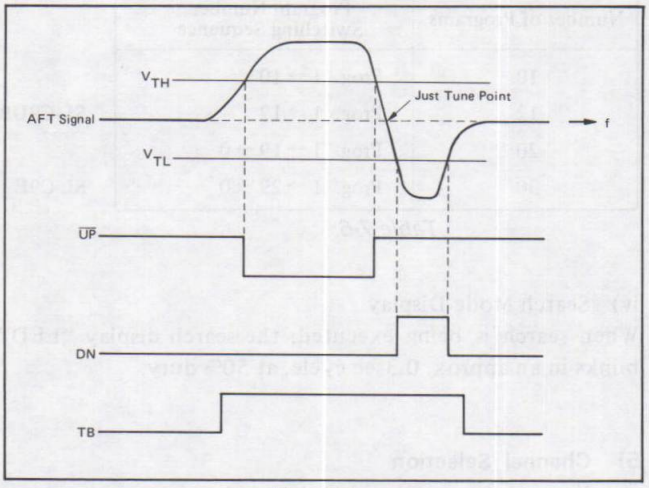


Fig. 7-7.

The digital AFT is controlled by input of UP or DN. The VHT is set at approx. 8.5V, and VTL is set at approx. 3.6V. (Q106, 107)

Also, the input of TB is assessed using a SYNC SEP signal (Q006). (Q103, 104)

11) D/A OUT Circuit

As described below, VC voltage data is stored as 14-bit digital data, and PWM output is obtained according to this data. The period "To" is divided into 64 small periods "Ts". The small period "Ts" is 256 times the minimum pulse width to = 555nS. When dividing 14-bit data into 6 bits on the LSB side and 8 bits on the MSB side, the data on the MSB side results in data indicating T1 ~ T64=nto. The data on the LSB side results in data indicating T1 ~ T64=12to (HEX MSB = OC: DEC MSB = 12) on the assumption that MSB=00001100 and LSB=000000.

Where LSB has been equal to 000001 by 1 bit count up, T32=13to, and the other results in 12to, the Increment will be "to".

When LSB has been equal to 000010 by the subsequent 1 bit count up, T16, T48=13to. Increment in this case is also "to".

When LSB has become 111111 is this way, T1 ~ T63=13to, and T64=12to. By the next 1 bit up, MSB=00001101 and LSB=000000resulting in T1 ~ T64=13to.

The difference is always "to", and repetitive periods equal approximately 7 kHz. The period To: Approx. 110 Hz.

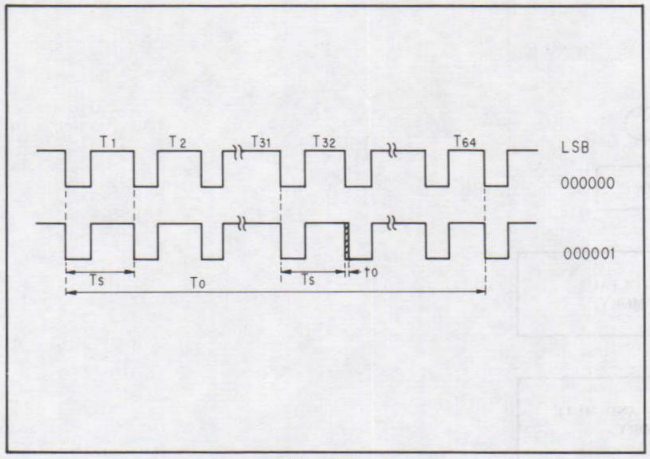


Fig. 7-8.

$LSB_{(EX)}$	Tn Longer by t0 (n=1–64)
000001	n = 32
000010	n = 16, 48
000100	n = 8, 24, 40, 56
001000	n = 4, 12, 20, 28, 36, 52, 60
010000	n = 2, 6, 10, ... , 58, 62
100000	n = 1, 3, 5, 7, ... , 61, 63

Table 7-9.

12) Prog. No. Display Output Port

P00 ~ P03 and P10 ~ P11 are output ports for prog. No. display. (N-ch transistor open drain) The lower digit of a prog. No. is output in a BCD code from the P00 ~ P03 statically, and the upper digit is output from the P10 ~ P11.

13) Function Stop Input

When $\overline{ST}$ input has been set to "L", the function of the M50118P stops, and the oscillator also stops. As a result, scan output stops, and the prog. No. display goes out. However, since the internal address counter maintaines the prog. No., by returning the $\overline{ST}$ to "H", the previous prog. No., which has been selected prior to $\overline{ST}$ is set to "L", and can be selected again.

If VDD has been set to "L", the address counter is reset, and the previous programming No. cannot be selected. Prog. No. "1" is automatically selected.

14) Auto-clear

By inserting a condenser between the $\overline{AC}$ terminal and VSS, "auto-clear" can be activated at power ON. For SL-C9E, reset time is 60mS or so owing to utilization of 1μF. Input is inhibited for approx. 128mS after "auto-clear" mode is activated.

15) Program Lock

When PR LOCK key has been input, channel selection by the key matrix is inhibited. Channel selection by a remote control timer is inhibited by each board. Program lock is required during the following operations;

1. REC. $\overline{PAUSE}$
2. TIMER REC
3. TIMER SET
4. TIMER REC reservation/confirmation

16) AFT Output Terminal

Mode	Output
Search	L
Search (Digital AFT)	Z
AFT ON	H
AFT OFF	Z

Z: High Impedance

Table 7-10.

17) MUTE Output Terminal

Mode	Output
AP	H
MUTE ON	Z
MUTE OFF	L

Z: High Impedance

Table 7-11.

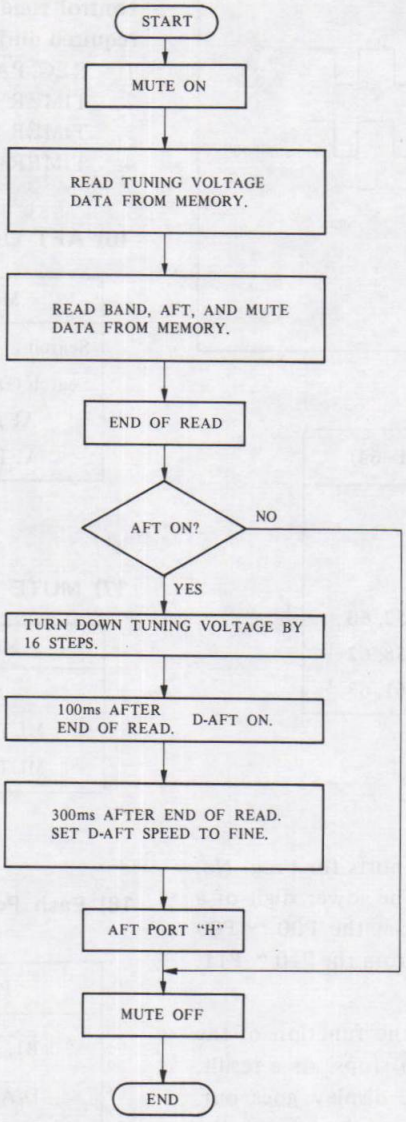
18) Each Port Output at Standby

Port	Output
$\overline{B1, B2}$	L
$\overline{D/A\ OUT}$	L
MUTE	Z
AFT	Z
I/O	Z
CLK, C1–C3	H
ϕ_A	H
ϕ_B–ϕ_D	L
$\overline{SD}$	Z
P00–P03	Z
P10–P11	L
OSC OUT	H

Z: High Impedance

Table 7-12.

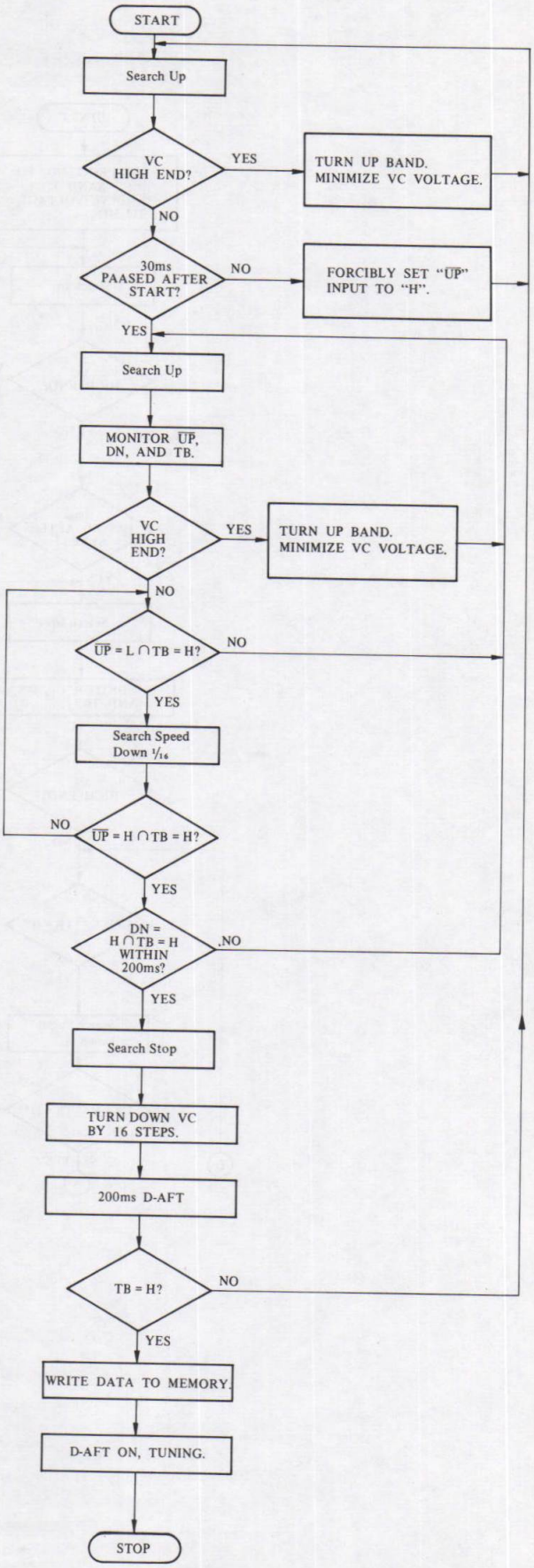
19) Channel Selection Flowchart



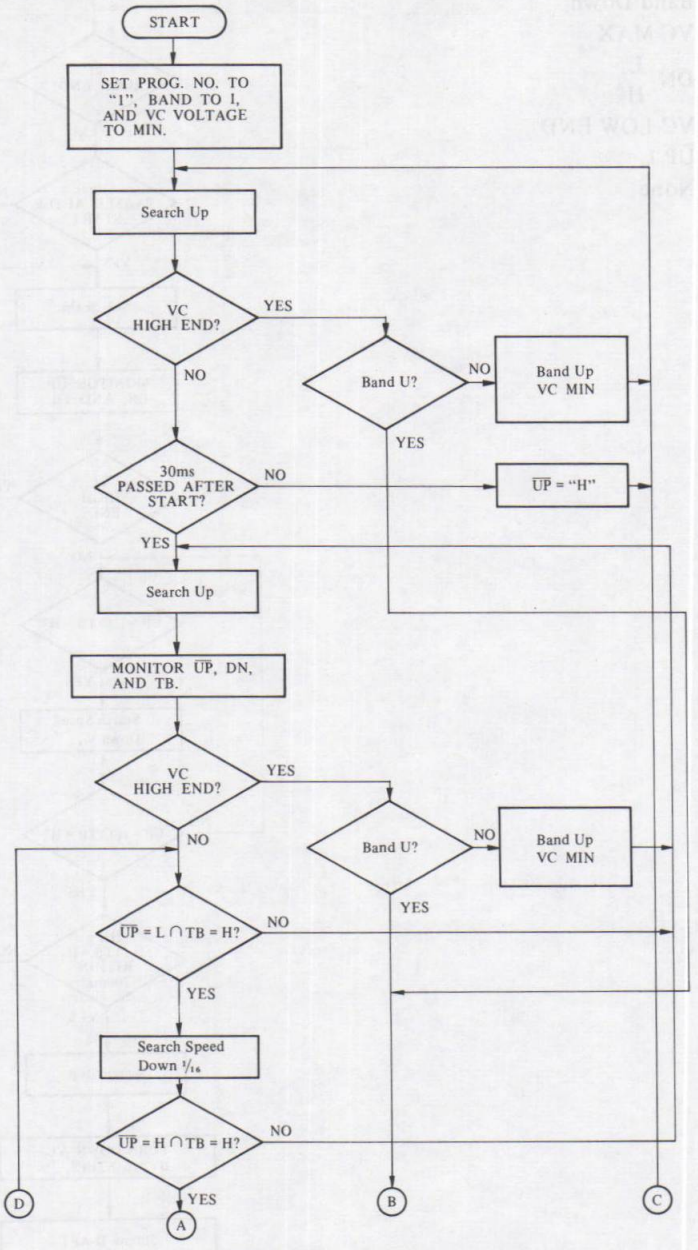
20) Search Up Flowchart

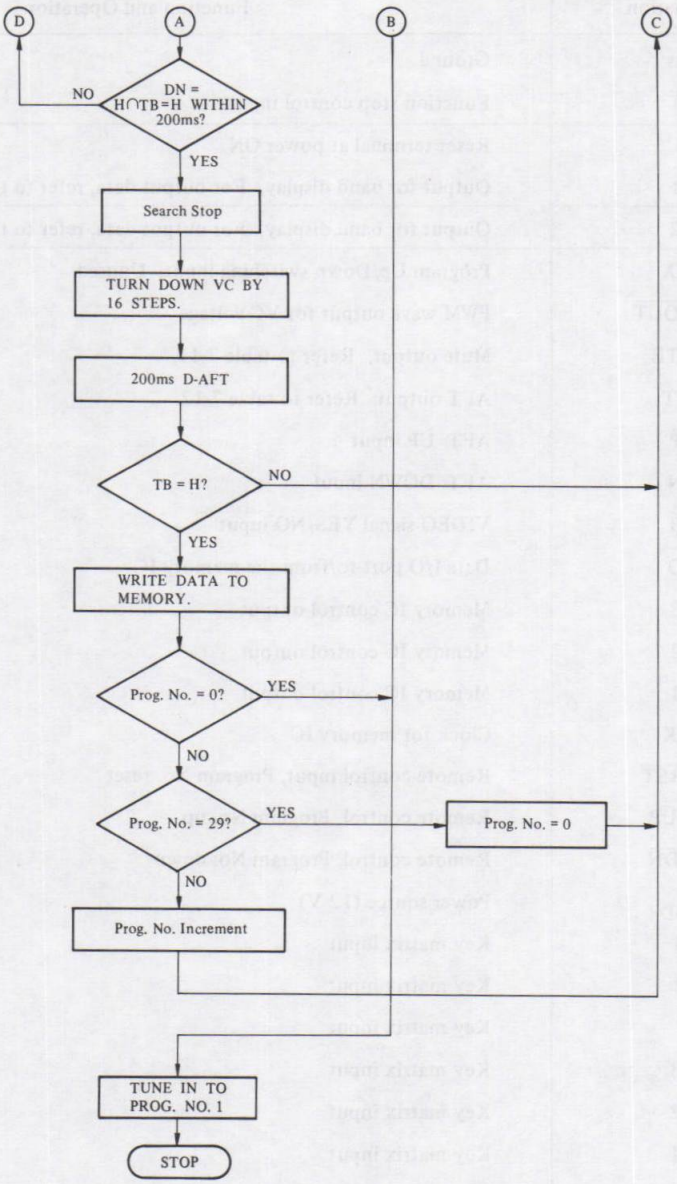
For "Search Down Flowchart", the contents in the "Search Up Flowchart" must be replaced as follows;

Search Up	→ Search Down
Band Up	→ Band Down
VC MIN	→ VC MAX
$\overline{UP}$ H / L	→ DN L / H
VC HIGH END	→ VC LOW END
DN H	→ $\overline{UP}$ L
16-Step Down	→ None



21) Automatic Programming Flowchart





22) IC101 (M50118P) Functions

M50118P		
Pin No.	Designation	Function and Operation
1	Vss	Ground
2	$\overline{ST}$	Function stop control input
3	$\overline{AC}$	Reset terminal at power ON
4	$\overline{B1}$	Output for band display. For output data, refer to table 7-7.
5	$\overline{B2}$	Output for band display. For output data, refer to table 7-7.
6	PFX	Program Up/Down switching input. Unused
7	$\overline{D/A\ OUT}$	PWM wave output for VC voltage
8	MUTE	Mute output. Refer to table 7-11.
9	AFT	AFT output. Refer to table 7-12.
10	$\overline{UP}$	AFT UP input
11	DN	AFT DOWN input
12	TB	VIDEO signal YES/NO input
13	I/O	Data I/O port to/from the memory IC
14	C3	Memory IC control output
15	C2	Memory IC control output
16	C1	Memory IC control output
17	CLK	Clock for memory IC
18	$\overline{PR\ RST}$	Remote control input, Program No. reset
19	$\overline{PR\ UP}$	Remote control, Program No. up
20	$\overline{PR\ DN}$	Remote control, Program No. down
21	V_{DD}	Power source (12 V)
22	I3	Key matrix input
23	I2	Key matrix input
24	I1	Key matrix input
25	K3	Key matrix input
26	K2	Key matrix input
27	K1	Key matrix input
28	PBEX	Program No./band No. of bands change-over input. Refer to table 7-2 and 7-3 for the input matrix.
29	$\overline{TEX}$	IC test input. Unused
30	ϕ_D	Key matrix scan output
31	ϕ_C	Key matrix scan output
32	ϕ_B	Key matrix scan output
33	ϕ_A	Key matrix scan output
34	$\overline{SD}$	Search mode display output
35	P11	Program No. upper digit displaying BCD code output.
36	P10	Program No. upper digit displaying BCD code output.
37	P3	Program No. lower digit displaying BCD code output.

Table 7-13. (1/2)

38	P2	Program No. lower digit displaying BCD code output.
39	P1	Program No. lower digit displaying BCD code output.
40	P0	Program No. lower digit displaying BCD code output.
41	OSC IN	External oscillator terminal
42	OSC OUT	External oscillator terminal

Table 7-13. (2/2)

A pull up or pull down resistance is provided concerning each of the following terminals:

Pull up resistance
(approx. 50kΩ) . . . . . $\overline{\text{PR RST}}$, $\overline{\text{PR UP}}$, $\overline{\text{PR DN}}$,
Pull up resistance $\overline{\text{UP}}$, DN, TB, $\overline{\text{TEX}}$
(approx. 100kΩ) . . . . . $\overline{\text{AC}}$
Pull down resistance
(approx. 50kΩ) . . . . . $\overline{\text{ST}}$, $\overline{\text{PFX}}$, I1 ~ I3,
K1 ~ K3, PBEX

7-2. OTHER IC FUNCTION DESCRIPTIONS (CHANNELS SELECTION)

1) M5G1400P

The M5G1400P is a non volatile MNOS IC of 14-bit 100 words, which is provided with a serial data I/O function.

IC102 (M5G1400P) Functions

M5G1400P		
Pin No.	Designation	Function and Operation
1	V_{SS}	Power source (+12 V)
2	V_{GG}	Power source (−24 V)
3	NC	
4	NC	
5	NC	
6	CLK	Clock input (14 kHz, "H" at standby)
7	C1	Mode control input. Refer to table 7-15.
8	C2	
9	C3	
10	NC	
11	NC	
12	I/O	Data I/O port Data structure is as follows: Tuning voltage 14 bits Band data 2 bits AFT ON/OFF 1 bit MUTE ON/OFF 1 bit } 18 bits Refer to Fig. 7-9 for the address data.
13	NC	
14	NC	

Table 7-14.

C1	C2	C3	Contents of command
H	H	H	Standby
H	H	L	Unused
H	L	H	Erase . . . . . The contents at a specified address are all set to "L."
H	L	L	Address accept . . . . . Address is transferred from the I/O port to the address register.
L	H	H	Read-out . . . . . The contents at a specified address are output to the data register.
L	H	L	Output . . . . . The contents of the data register are output to the I/O port.
L	L	H	Write-in . . . . . The contents of the data register are stored to a specified address.
L	L	L	Data accept . . . . . Data is transferred from I/O device to data register.

Table 7-15.

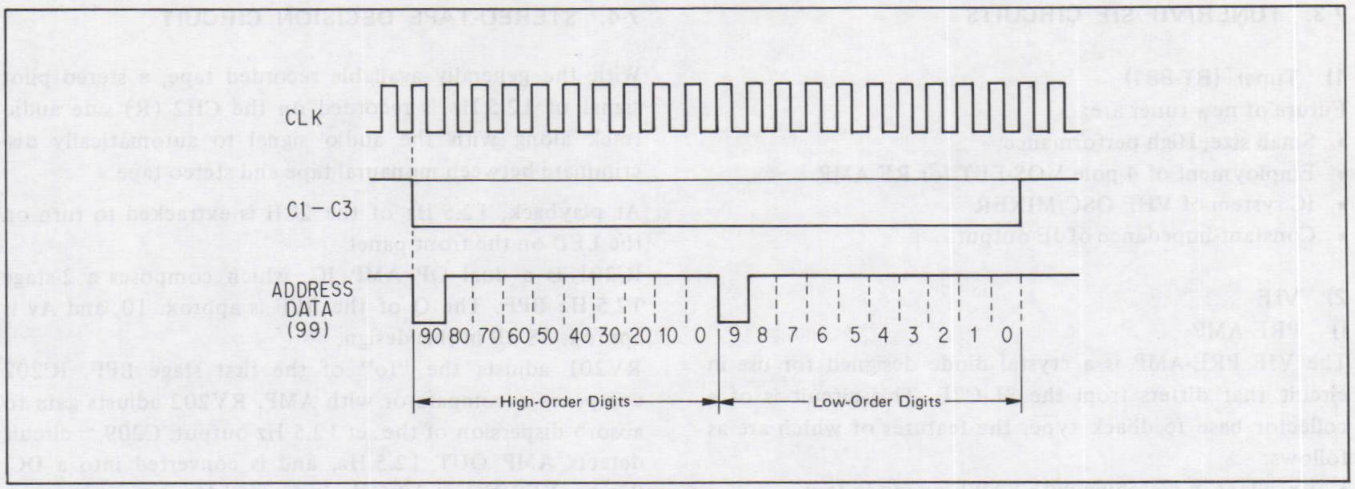


Fig. 7-9.

2) M54570L

The M54570L is a band switching IC. (4 bands) Two states are available for the input terminal "H" voltage, which realizes connection with various tuners. Also, since the withstand voltage of the output terminal is a max. 26V, connection with a tuner requiring negative voltage for the band switch is possible.

3) μPC574J

The μPC574J is a high stable and constant-voltage IC with the VC reference voltage being 33V. Temperature coefficient is ±1.0 mV/°C.

IC104 (M54570L) Functions

M54570L		
Pin No.	Designation	Function and Operation
1	O3	Band output 3
2	O1	Band output 1
3	IN B	Input B
4	IN A	Input A
5	GND	Ground
6	O4	Band output 4
7	O2	Band output 2
8	V_{CC}	Power source (+12 V)

Table 7-16.

Band *1	IN A	IN B	O1	O2	O3	O4
U	L	L	H	H	L	H
	L	H	L	L	H	L
	H	L	H	H	L	L
	H	H	H	L	L	L
I	H*	H*	H	L	L	H
III	H*	L	H	H	L	L

Table 7-17.

Input
L = 0.4 V MAX
H = 4 V – 10 V
H*= 10 V MIN

Output
L = Tr. OFF (OPEN)
H = Tr. ON (V_{CC})

*1: SL-C9E

7-3. TUNER/VIF/SIF CIRCUITS

1) Tuner (BT-881)

Future of new tuner are:

- Small size, High performance
- Employment of 4-pole MOS-FET for RF AMP
- IC system of VHF OSC/MIXER
- Constant-impedance of IF output

2) VIF

i) PRE-AMP

The VIF PRE-AMP is a crystal diode designed for use in circuit that differs from the SL-C7E. This circuit is of a collector base feedback type, the features of which are as follows:

- Excellent in matching with SAWF owing to low
- output impedance (100Ω or less)
- AMP gain can be changed by altering the feedback resistance.
- AMP collector output circuit need not be adjusted.

ii) SAWF

F-1034 is used instead of the F-1024. This F-1034 is differs from F-1024 regarding the following points:

- Insertion loss is decreased by 3 ~ 4 dB.
- Trap performance for channel adjustment has been improved.
- There is a dent near the center of the passing band.

3) VIF IC

TA7660P is employed.

This differs from TBA1440G of SL-C7E regarding the following points:

- Reverse AGC
- From keyed AGC to peak AGC
- Detective output level is fixed to 2.6 Vp-p type.

The detector is of a synchronous detection system, in the same way as with TBA1440G. The major point of difference is that the AFT circuit is built into the IC.

4) SIF

μPC1391H is employed for the SIF IC.

Features are as follows:

- Realization of non-adjustment
- Excellent in AMR characteristics

i) Input filter

A ceramic filter is employed to realize non-adjustment.

ii) Discriminator

A ceramic discriminator is employed to realize non-adjustment.

iii) Audio mute

Sufficient effect of audio mute cannot be obtained on the TU-24 board. For this reason, a muting signal is transmitted to the AM-1 board for audio mute purposes.

7-4. STEREO-TAPE DECISION CIRCUIT

With the generally available recorded tape, a stereo pilot signal of 12.5·Hz is recorded on the CH2 (R) side audio track along with the audio signal to automatically discriminate between monaural tape and stereo tape.

At playback, 12.5 Hz of the 2CH is extracked to turn on the LED on the front panel.

IC201 is a dual OP AMP IC, which composes a 2-stage 12.5 Hz BPF. The Q of the BPF is approx. 10, and Av is approx. 38 dB in this design.

RV201 adjusts the "fo" of the first stage BPF. IC202 composes a comparator with AMP. RV202 adjusts gain to absorb dispersion of the set 12.5 Hz output. C209 ~ circuit detects AMP OUT 12.5 Hz, and is converted into a DC. Source YES/NO of 12.5 Hz is decided by the comparator, and the corresponding LED is turned on.

7-5. TIMER BACKUP CIRCUIT

In the event of a power failure, the timer can be operated by means of a backup circuit BA301 Ni-Cd battery power source, charged by the R301. The DC-DC converter of Q301/T301 terminates oscillation.

Where a power failure occurs, oscillation of Q301/T301 occurs and 5V is generated at pin 1 of CN102. By charging for about 30 hours by means of the Ni-Cd battery enables about a 10-minute backup.

SECTION 8
MECHANICAL OPERATION

8-1. CASSETTE INSERTION AND THREADING

Figs. 8-1 ~ 8-4 show the cassette mechanism and operation of mechanical components in the cassette compartment assembly. When the power is turned on, the drum motor rotates clockwise momentarily. When a cassette is inserted, section Ⓐ of the cassette passes claw ② on cassette compartment assembly ①, the lock mechanism inside the cassette is released, and claw ③ is pushed in. Cassette lid ④ is pushed up in the direction of the arrow at cassette compartment assembly ① section Ⓑ, and is opened completely by lid opener ⑤.

Pin ⑥ on cassette lid ④ rotates in the direction of arrow Ⓒ when the lid opens up. Claws ⑦, ⑦' rotate in the direction of Ⓓ around shaft ⑧ and the tape gear ⑨ locks are released. The release of these gears allows supply reel ⑩ and take-up ⑪ to rotate freely.

When the cassette is pushed in further, section Ⓐ comes into contact with section Ⓔ, C slide plate (L) ⑫ and C slide plate (R) ⑬ move in the direction of the arrow, C-IN cam (L) ⑭ and (R) ⑮ rotate, and microswitches ⑯, ⑰ turn on.

This causes FL motor ⑱ to operate, and worm gear ⑲ rotates in the direction of the arrow. This rotation causes worm wheel ⑳ and gear A ㉑ to rotate respectively in the directions of the arrows. The rotation of gear A ㉑ causes sector gear ㉒ and holder drive arm ㉓ to rotate in the direction of the arrow, and cassette compartment assembly ① containing the cassette begins to move in the direction of arrow Ⓕ. Gears B ㉔ and E ㉕ on cassette compartment assembly ① rotate in the direction of the arrow along rack (L) ㉖ and (R) ㉗, respectively, and cassette compartment assembly ① is set in position. Gears Ⓒ ㉘, ㉙ also rotate in the direction of the arrow. When cassette compartment assembly ① drops and guide roller ㉚ pushes lock stopper ㉛ section Ⓖ down, section Ⓗ lock is released. Lock plate ㉜ moves in the direction of the arrow, rotating unlock lever ㉝ in the direction of the arrow. The rotation of unlock lever ㉝ causes unlock

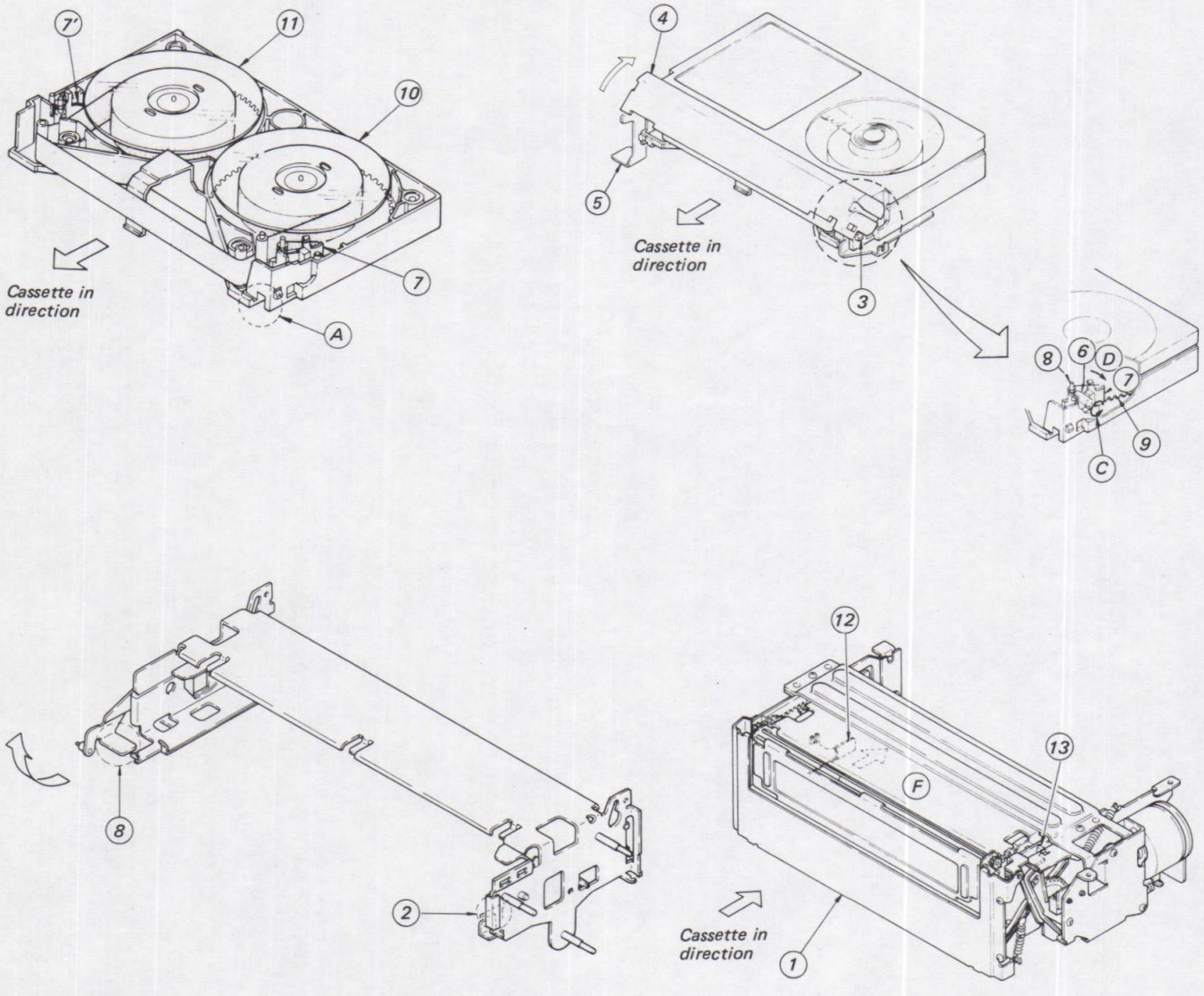


Fig. 8-1.

link plate (34) and unlock plate (35) to move in the direction of the arrow. CD adjustment plate (36) moves in the same direction as lock plate (32), and microswitch (37) turns on. FL motor (18) stops, threading motor (38) turns on, and threading operation begins.

The movement of cassette compartment assembly (1) causes door arm (L) (39) and arm (R) (40) to rotate respectively in the directions of the arrows, and tension coil springs (41), (42) move cassette door assembly (43) in the direction of the arrow. The operation of microswitches (16), (17) energizes brake solenoid (44) which is between the two reel motors. Brake arm (45) moves in the direction of the arrow, the supply reel (46) and take-up reel (47) brakes are released, and supply reel (48) moves in the direction of the arrow to send tape out. However, in order for supply reel (48) to maintain back tension on the tape, power is actually applied in the direction opposite to that shown in the diagram, and tape tension causes rotation in the direction illustrated. At this time, take-up reel (49) is braked electrically and does not rotate. With the rotation of the supply reel, threading motor (38) rotates in the direction of the arrow. This rotation is transmitted to gear assembly (50) via the belt, and the gears rotate respectively in the directions of the arrows. These gears cause S threading ring (51) and slider gear assembly (52) to rotate respectively in the directions of the arrows.

The loading shuttle assembly (53) on S threading ring (51), No. 2 guide (54) and No. 3 guide (55) guide the tape to the prescribed position. No. 2 guide (54) and No. 3 guide (55) are inside pin recliner (56), and are contrived so that they rise up with the rotation of S threading ring (51).

When S threading ring (51) begins to rotate, the movement of cut-out section (I) causes unthreading end switch arm assembly (57) to move in the direction of the arrow, pushing the unthreading end switch actuator, and the switch operates. When S threading ring (51) reaches the prescribed position, lock arm assembly (58) lock roller drops into section (J), lock arm assembly (58) moves in the direction of the arrow, and threading end switch (59) turns off.

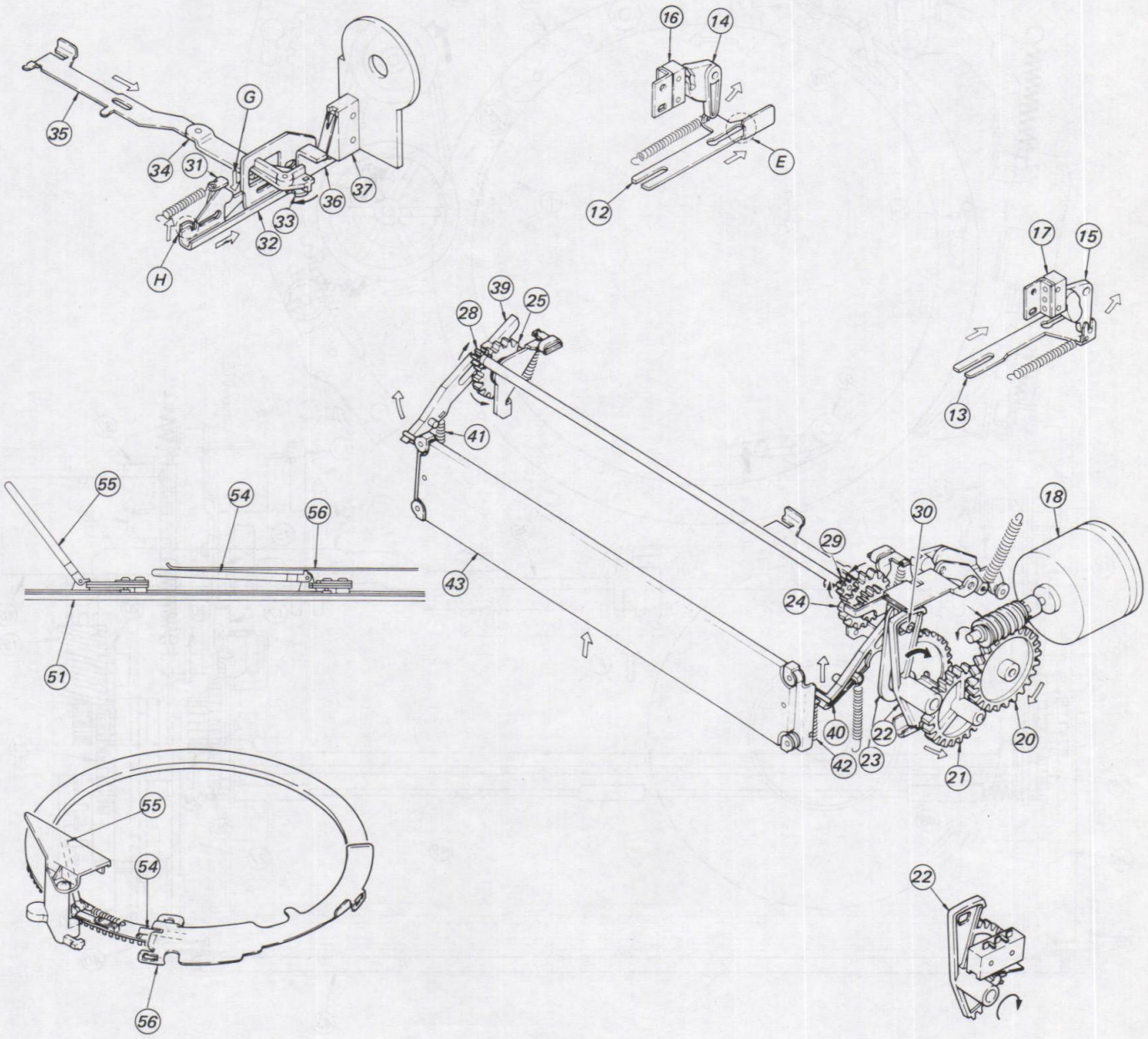


Fig. 8-2.

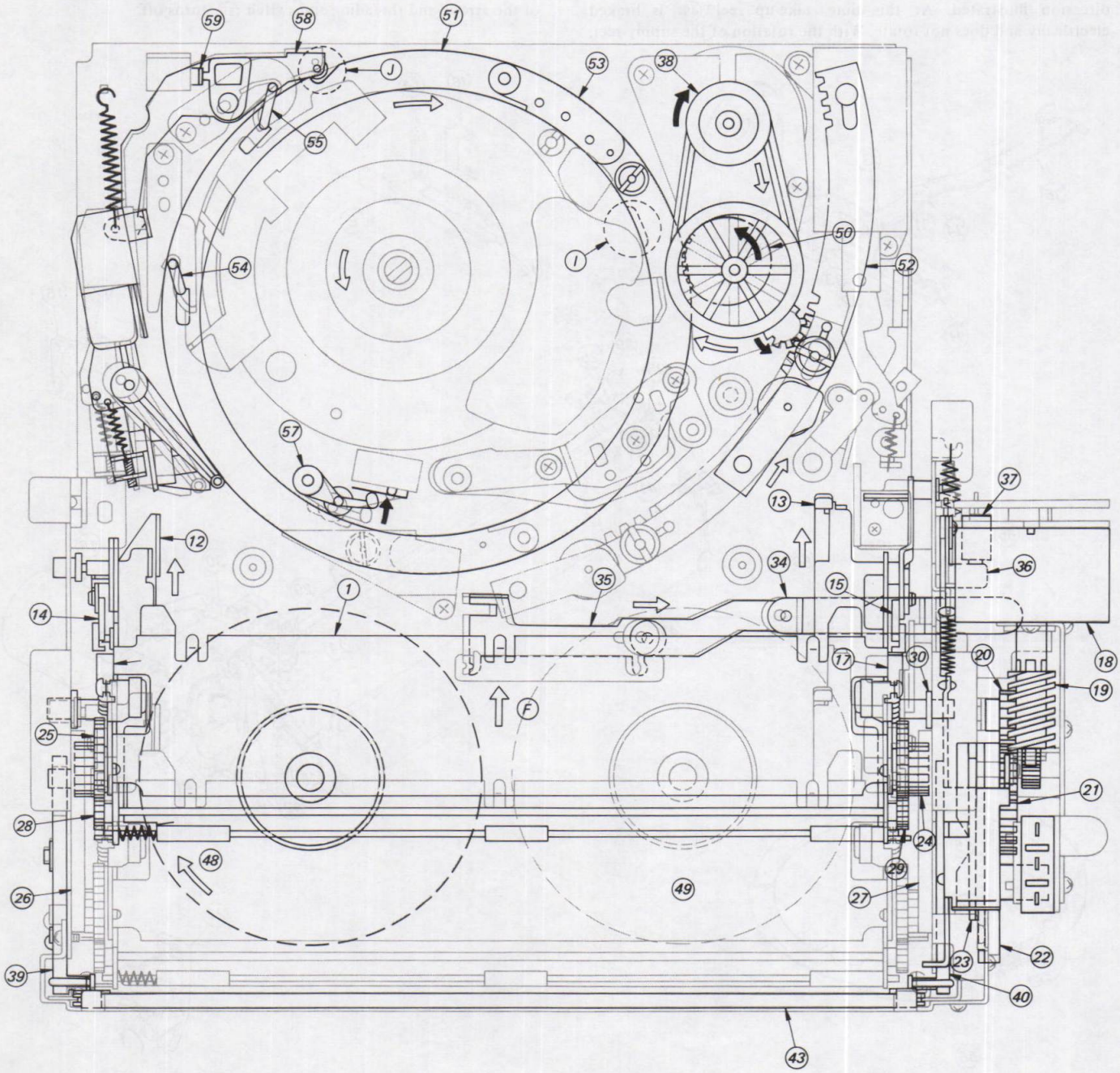
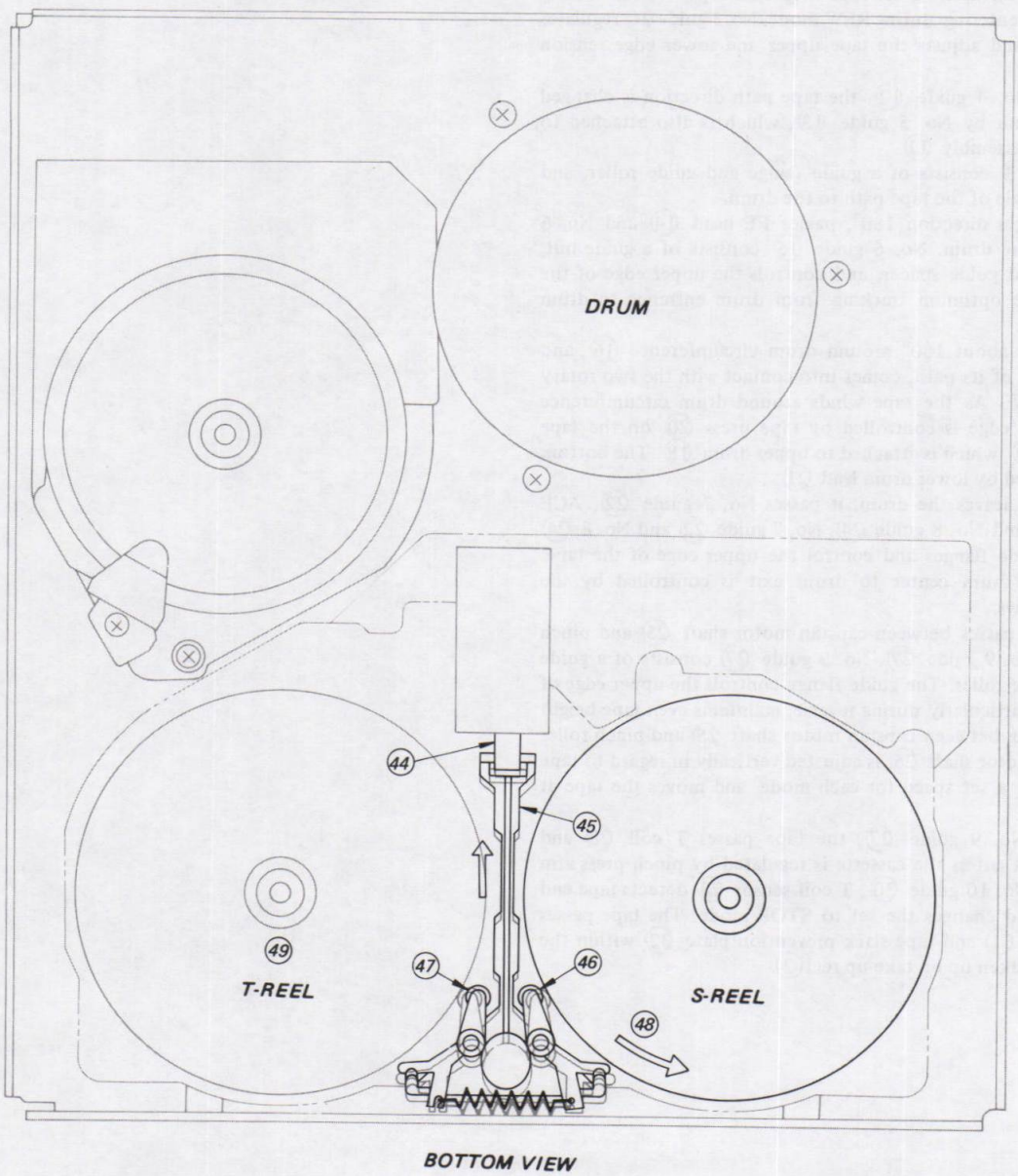


Fig. 8-3.



BOTTOM VIEW

Fig. 8-4.

8-2. TAPE PATH

Fig. 8-5 illustrate the tape path from supply reel. ① to take-up reel ②.

The tape which leaves supply reel ① passes guide ③, tape slack prevention plate ④ and exit guide ⑤ within the cassette and is pulled out.

Tape which has slack within the cassette will be damaged if pulled out, so tape slack prevention plate ④ prevents this slackness.

The tape passes S coil sensor ⑧ on TP base assembly ⑦ via No. 1 guide ⑥. When the tape is completely taken up on take-up reel ②, this S coil sensor ⑧ detects the metallic section at tape end, changing from the mode (PLAY, FF, REC, etc.) to STOP mode, immediately changing automatically to REW mode.

After passing S coil sensor ⑧, the tape passes No. 2 guide ⑨, No. 3 guide ⑩ and comes to No. 4 guide ⑫ which is attached to loading shuttle assembly ⑪.

No. 2 guide ⑨ maintains a set tape height for tape which is leaving the cassette, or entering during REW mode. No. 3 guide ⑩ regulates tape direction and adjusts the tape upper and lower edge tension balance.

After passing No. 4 guide ⑫, the tape path direction is changed toward the drum by No. 5 guide ⑬, which is also attached to loading shuttle assembly ⑪.

No. 5 guide ⑬ consists of a guide flange and guide roller, and regulates the angle of the tape path to the drum.

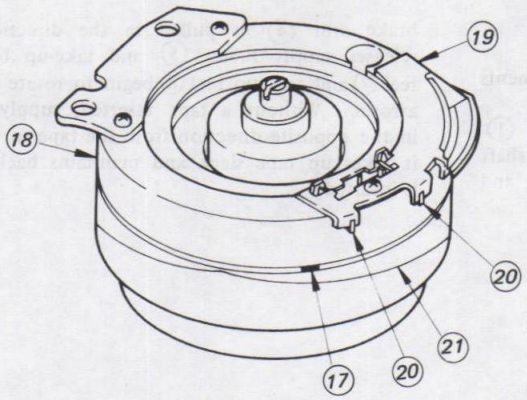
The tape changes direction 180°, passes FE head ⑭ and No. 6 guide ⑮ to the drum. No. 6 guide ⑮ consists of a guide nut, guide flange and guide spacer, and controls the upper edge of the tape to provide optimum tracking from drum entrance to drum center.

The tape winds about 180° around drum circumference ⑯, and during this part of its path, comes into contact with the two rotary video heads ⑰. As the tape winds around drum circumference ⑯, the upper edge is controlled by tape press ⑳ on the tape press holder ⑲, which is attached to upper drum ⑱. The bottom edge is controlled by lower drum lead ㉑.

When the tape leaves the drum, it passes No. 7 guide ㉒, ACE assembly ㉓, and No. 8 guide ㉔. No. 7 guide ㉒ and No. 8 ㉔ guides have guide flanges and control the upper edge of the tape. Tracking from drum center to drum exit is controlled by the adjustment screws.

Next, the tape passes between capstan motor shaft ㉕ and pinch roller ㉖ to No. 9 guide ㉗. No. 9 guide ㉗ consists of a guide flange and guide roller. The guide flange controls the upper edge of the tape, and particularly during reverse, maintains even tape height for tape entering between capstan motor shaft ㉕ and pinch roller ㉖. Capstan motor shaft ㉕ is adjusted vertically in regard to tape path, rotates at a set speed for each mode, and moves the tape at a set velocity.

After passing No. 9 guide ㉗, the tape passes T coil ㉘ and tape height as it enters the cassette is regulated by pinch press arm assembly ㉙ No. 10 guide ㉚. T coil sensor ㉘ detects tape end during REW and changes the set to STOP mode. The tape passes entrance guide ㉛ and tape slack prevention plate ㉜ within the cassette and is taken up on take-up reel ②.



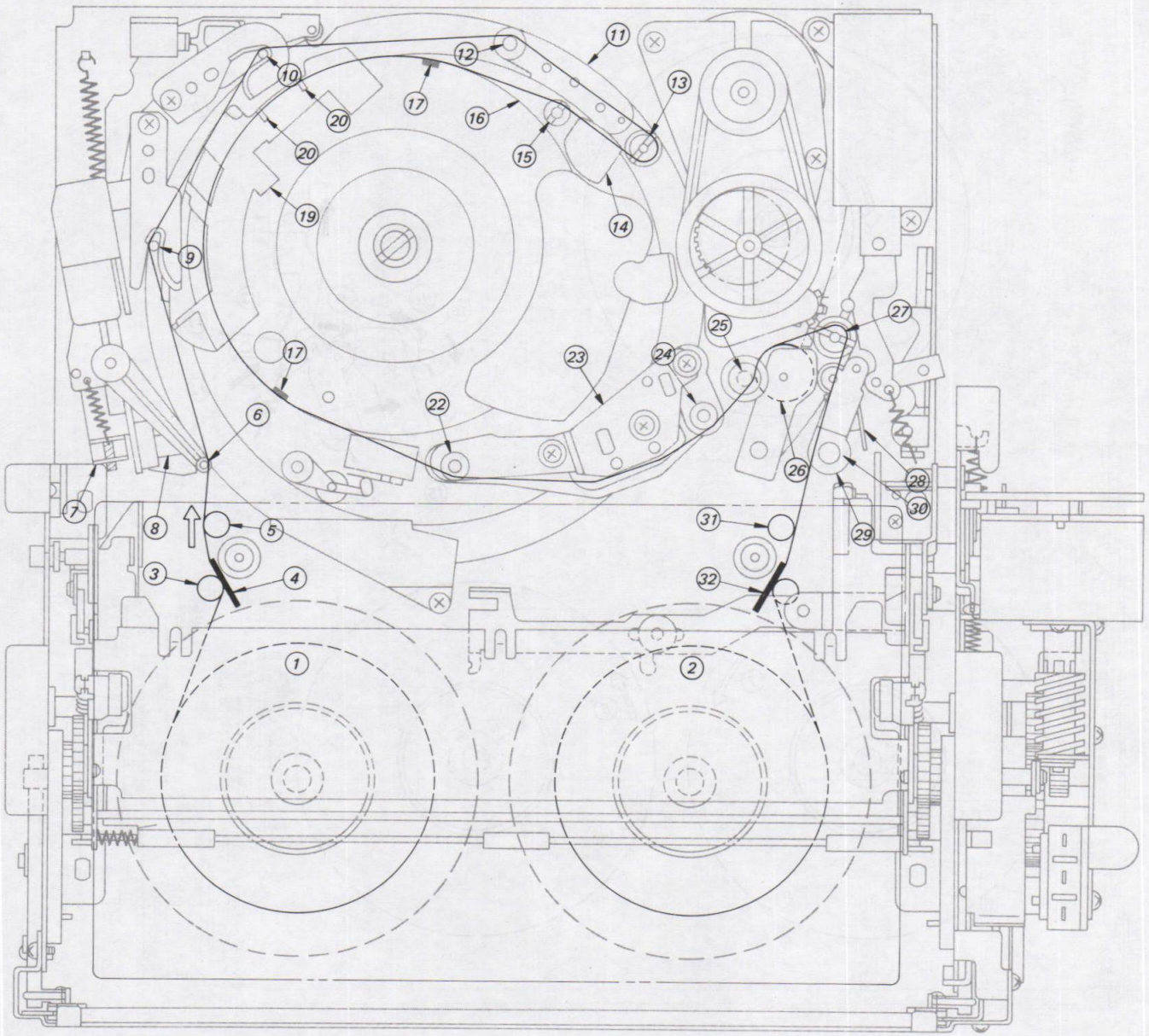


Fig. 8-5.

8-3. PLAY MODE

Figs. 8-6, 7 show the operation of the mechanical components during PLAY mode.
When the PLAY button is pressed, the drum motor drum ① rotates in the direction of the arrow, as does capstan motor shaft ②. Brake solenoid ③ on the reel motor board activates, and brake arm ④ is pulled in the direction of the arrow. This releases supply brake ⑤ and take-up brake ⑥, and supply reel ⑦ and take-up reel ⑧ begin to rotate in the direction of the arrows. Without a tape inserted, supply reel motor ⑦ rotates in the opposite direction from the tape forward direction, because it takes up tape slack and maintains back tension when a tape is inserted.

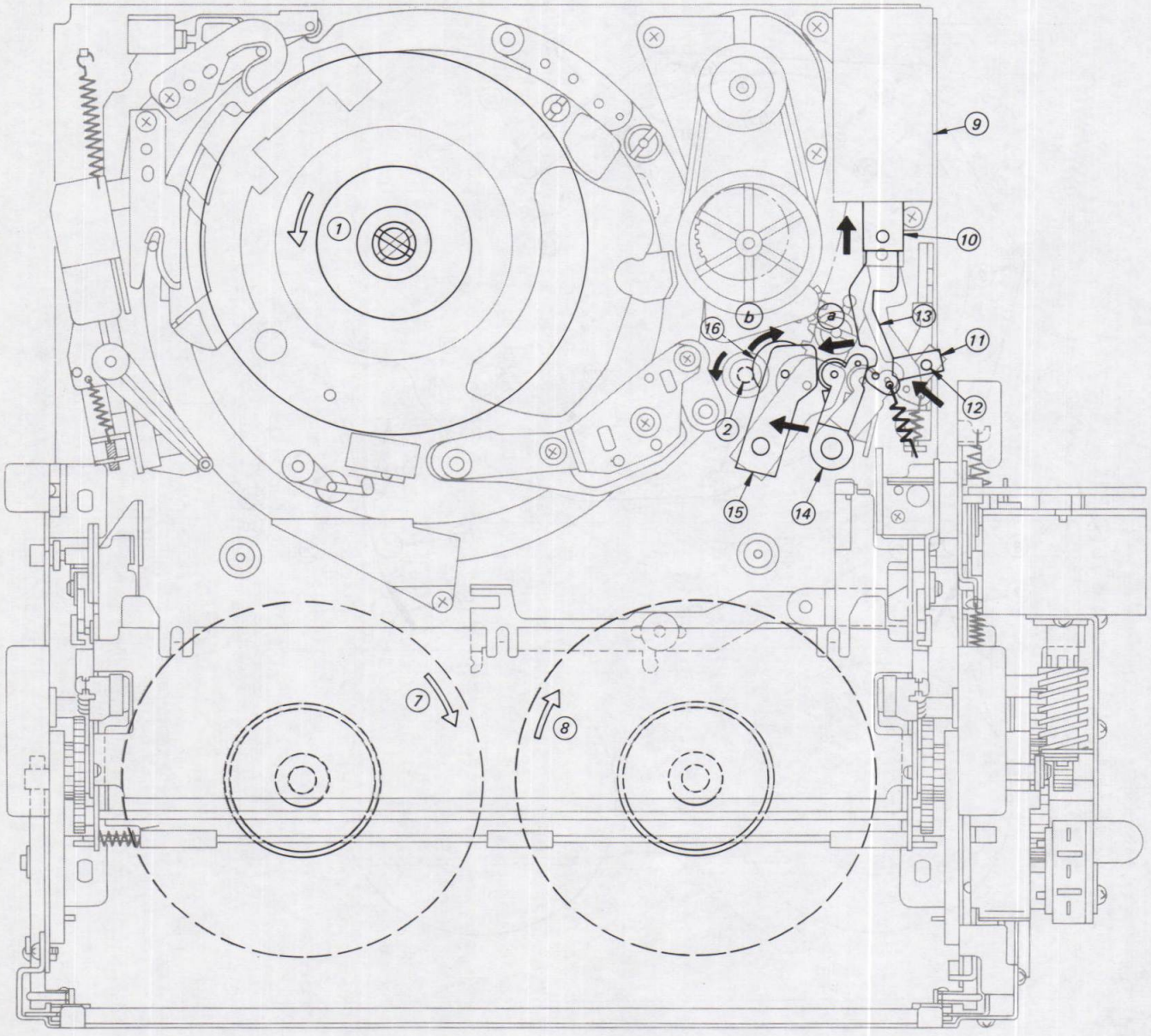
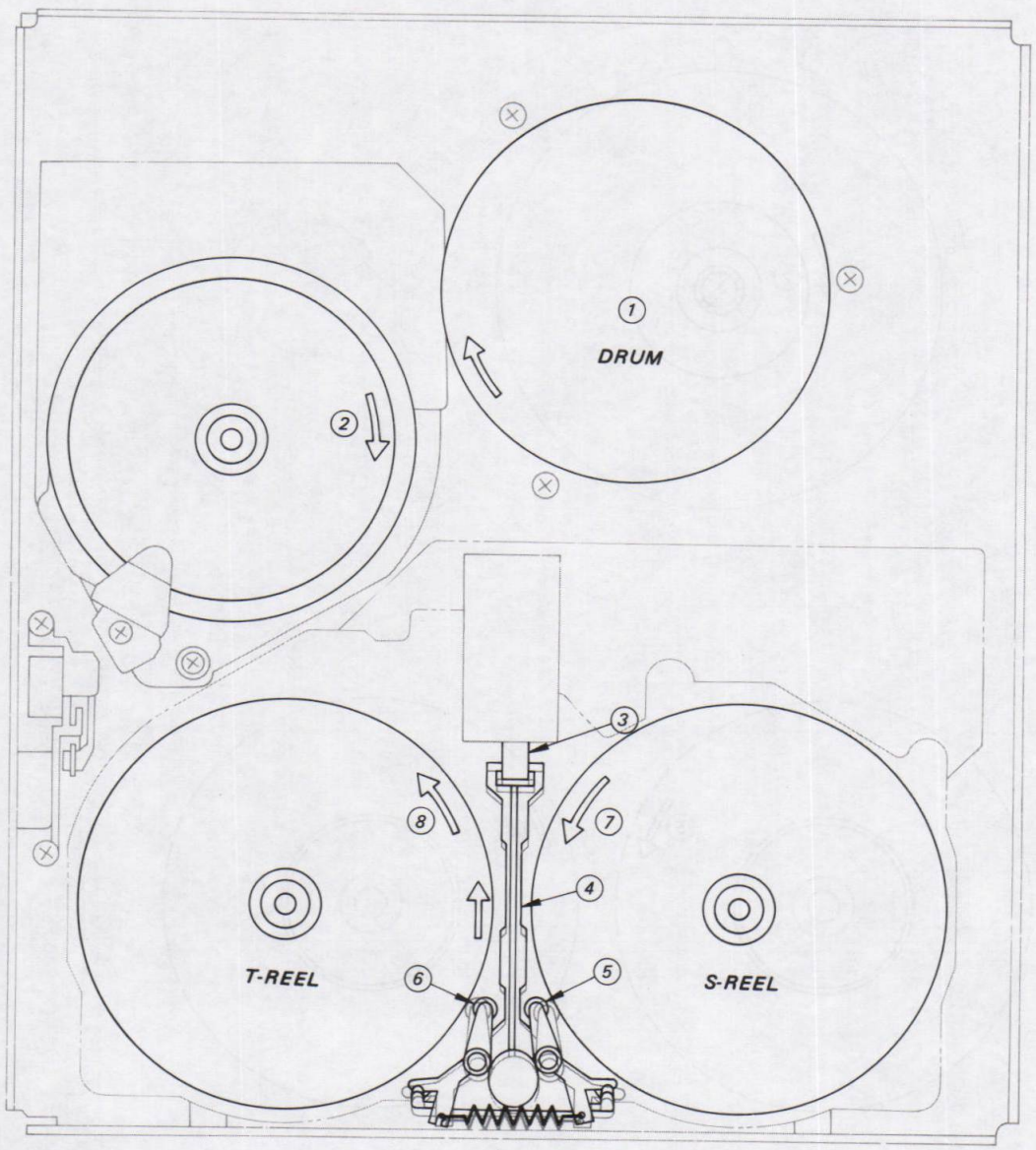


Fig. 8-6.

the tape forward transportation direction, because it takes up tape slack and maintains back tension when there is a tape inserted.
Pinch solenoid ⑨ energizes plunger ⑩, and PL link ring ⑪ rotates around shaft ⑫ in the direction of the arrow, pushing pinch solenoid arm ⑬ in the direction of arrow ⓐ. Arm ⑬ pushes pinch press arm ⑭ in the same direction, and pinch roller arm assembly ⑮ pushes the tape against capstan motor shaft ②. Pinch roller ⑯ on pinch roller arm assembly ⑮ rotates in the direction of arrow ⓑ according to the rotation of capstan motor shaft ②, and moves the tape toward the T-reel.



BOTTOM VIEW

Fig. 8-7.

8-4. FF MODE

Figs. 8-8, 9 show FF mode operation.
When the FF button is pressed, brake solenoid ① is energized, and brake arm ② is pulled in the direction of the arrow. This releases supply brake ③ and take-up brake ④, and take-up reel ⑥ begins to rotate. Supply reel ⑤ rotates in the same direction as the tape is taken up on take-up reel ⑥.
At the same time, the drum ⑦ rotates respectively in the directions of the arrows. The above operation is shown in Fig. 8-9 as seen from the back of the mech chassis.

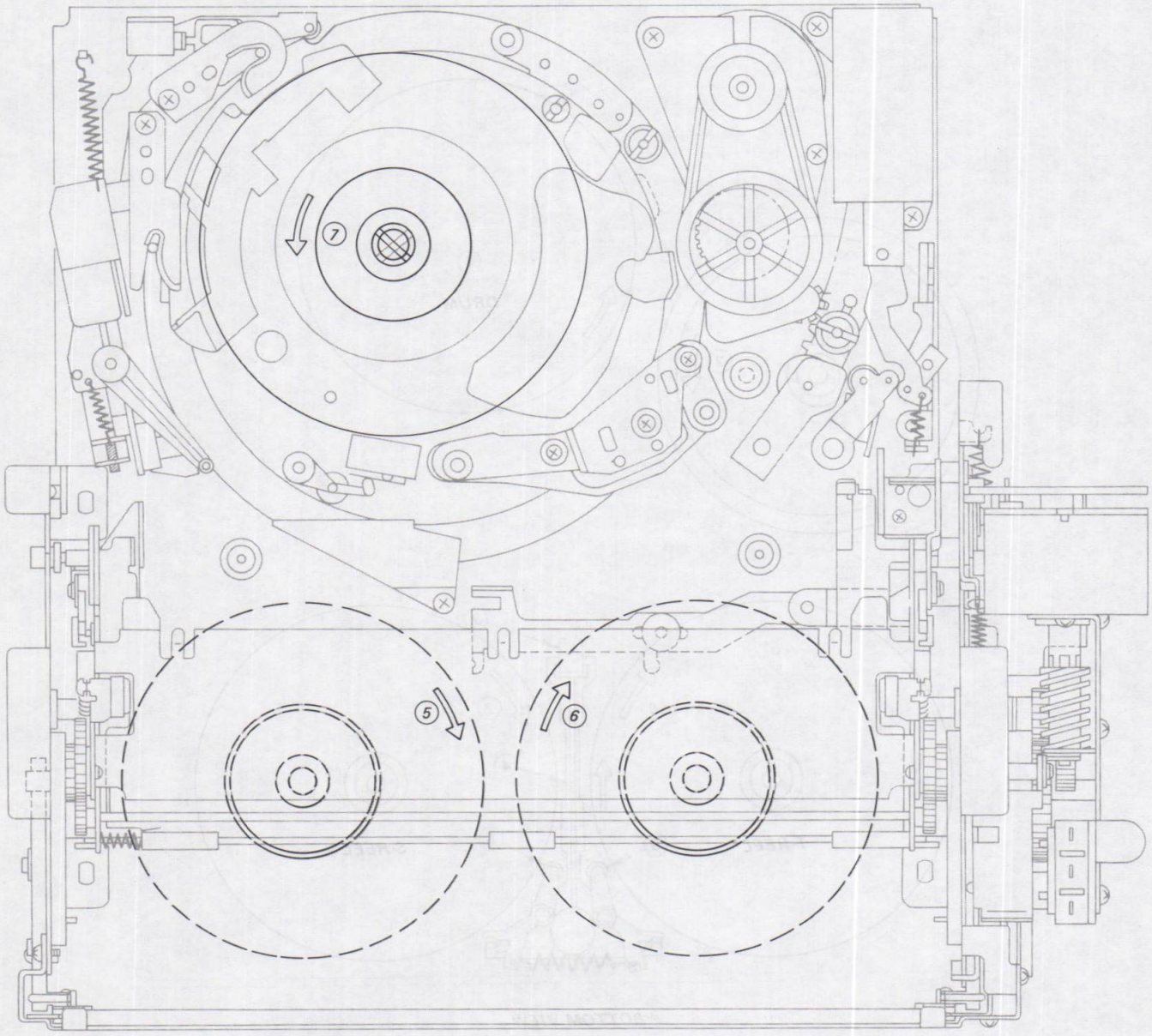
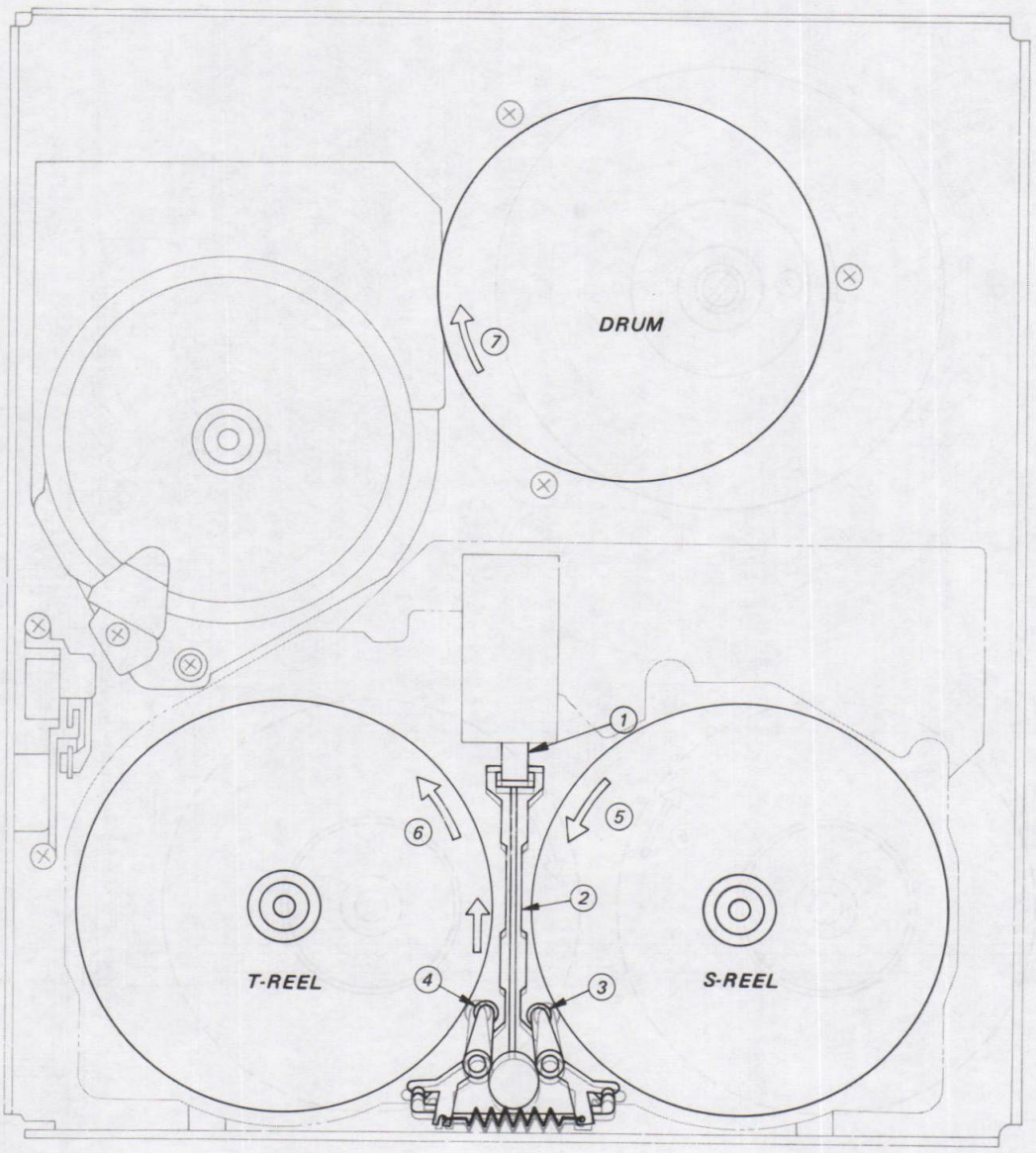


Fig. 8-8.



BOTTOM VIEW

Fig. 8-9.

8-5. REW MODE

Figs. 8-10, 11 show REW mode operation. When the REW button is pressed, brake solenoid (1) is energized, and brake arm (2) is pulled in the direction of the arrow. This releases supply brake (3) and take-up brake (4), and REW operation begins.

In REW mode, supply reel (5) rotates in the opposite direction from FF mode rotation, and take-up reel (6) rotates in the same direction as tape is taken up on supply reel (5). At the same time, the drum (7) rotates respectively in the directions of the arrows. The above operation is shown in Fig. 8-11 as seen from the back of the mech chassis.

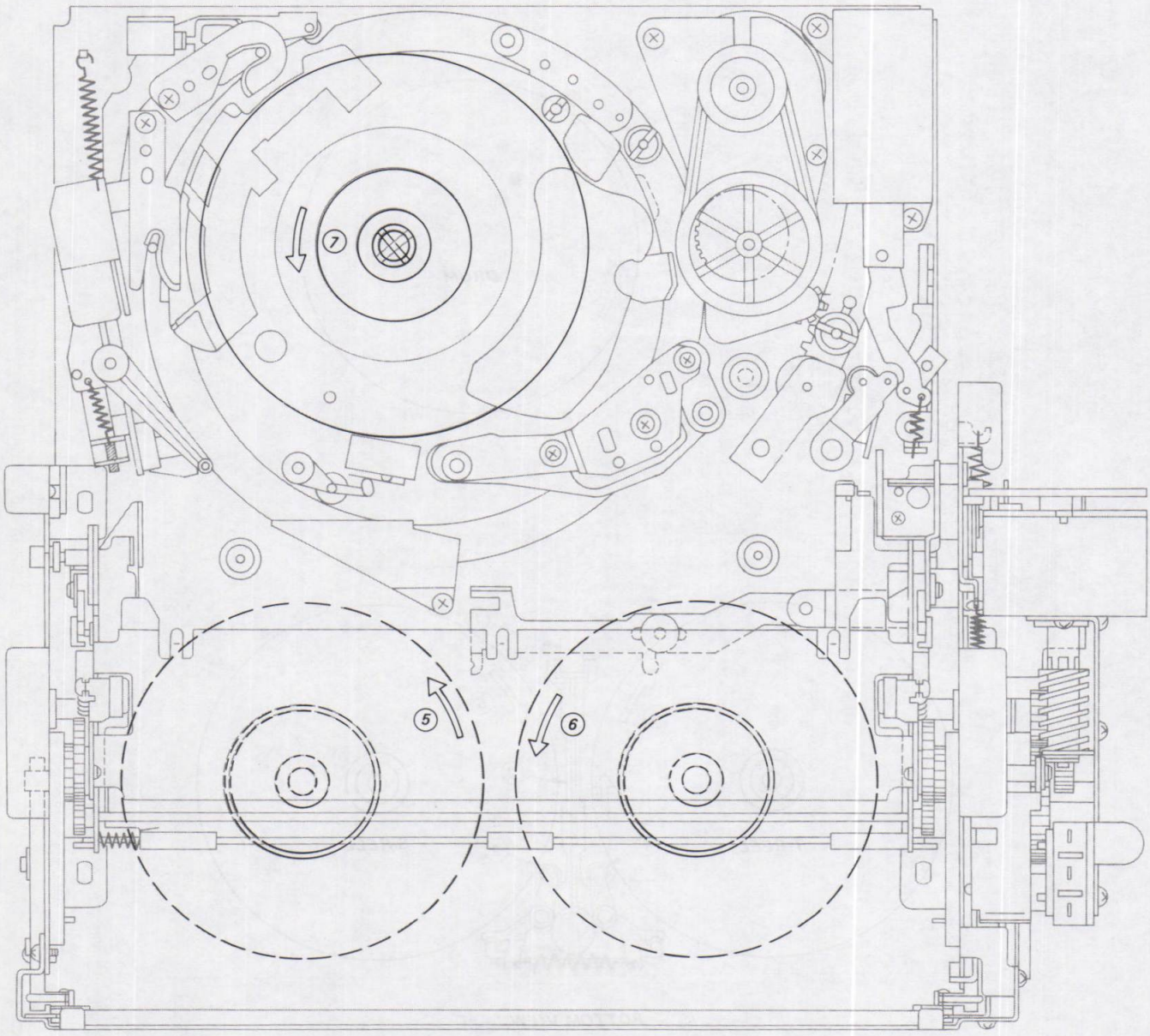
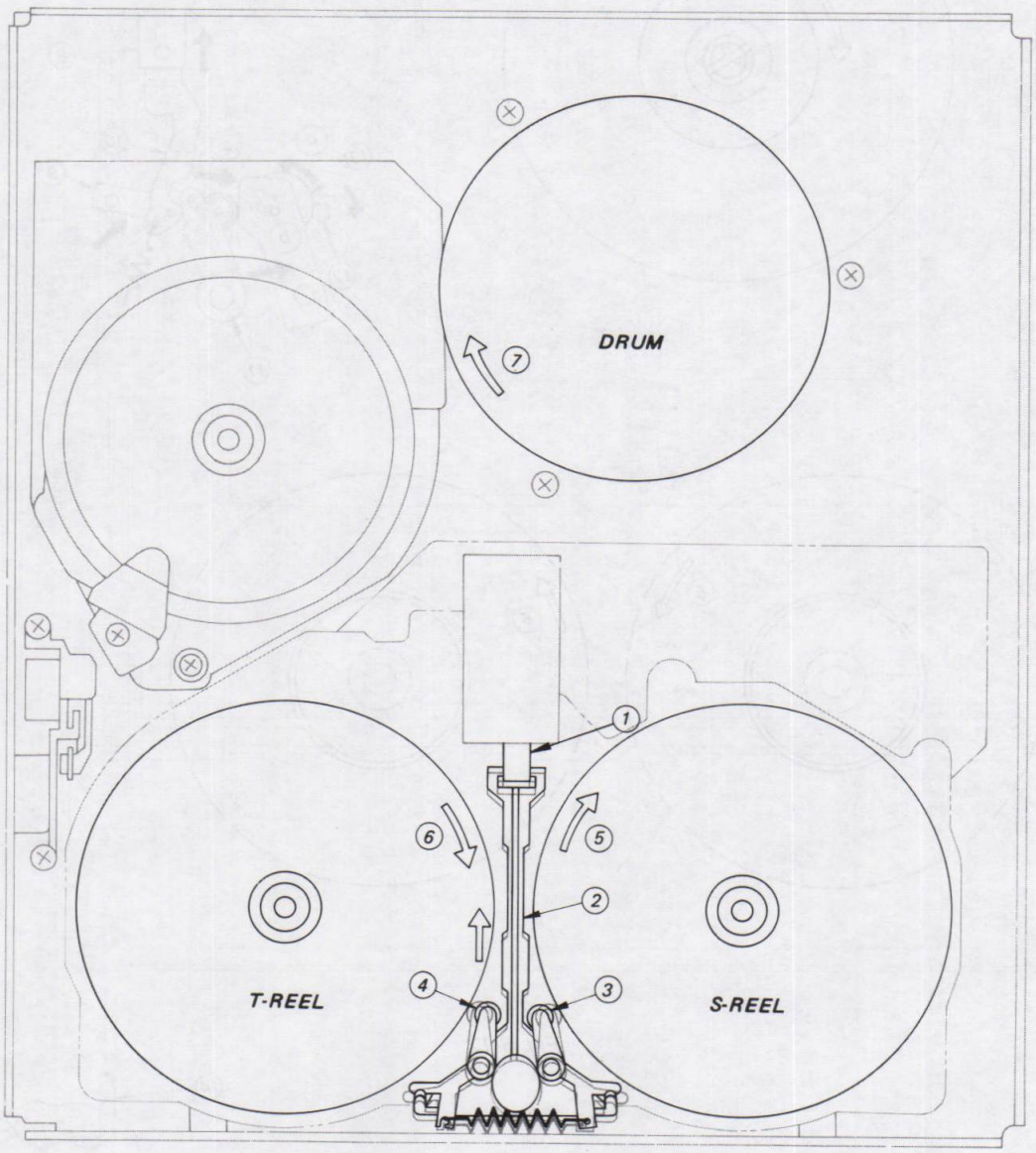


Fig. 8-10.



BOTTOM VIEW

Fig. 8-11.

8-6. REC MODE

By depressing the REC key the REC mode can be selected.
Figs. 8-12, 13 show the mechanical operation during REC mode.
Brake solenoid (1) is energized, and brake arm (2) moves in the direction of the arrow, releasing supply brake (3) and take-up brake (4). Supply reel (5) and take-up reel (6) begin to rotate. At the same time, pinch solenoid (7) is energized, plunger (8) is pulled in the direction of the arrow, PL link ring (9) rotates in the direction of the arrow, and pinch solenoid arm (10) is pushed in the direction of

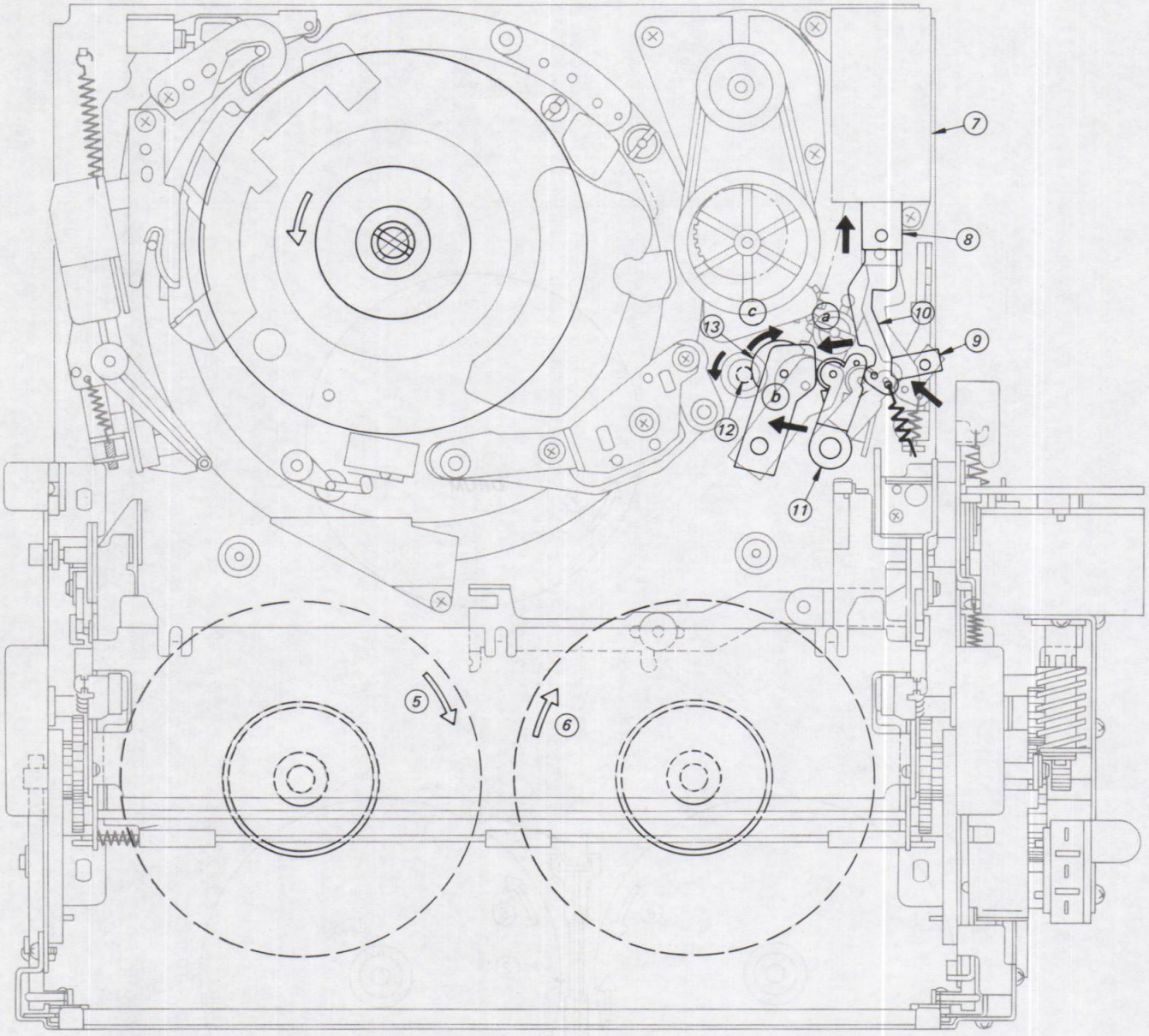


Fig. 8-12.

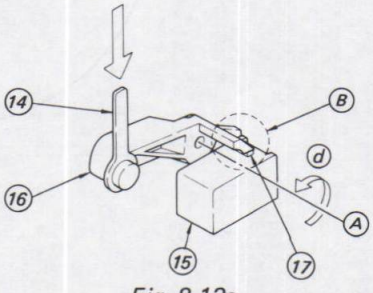


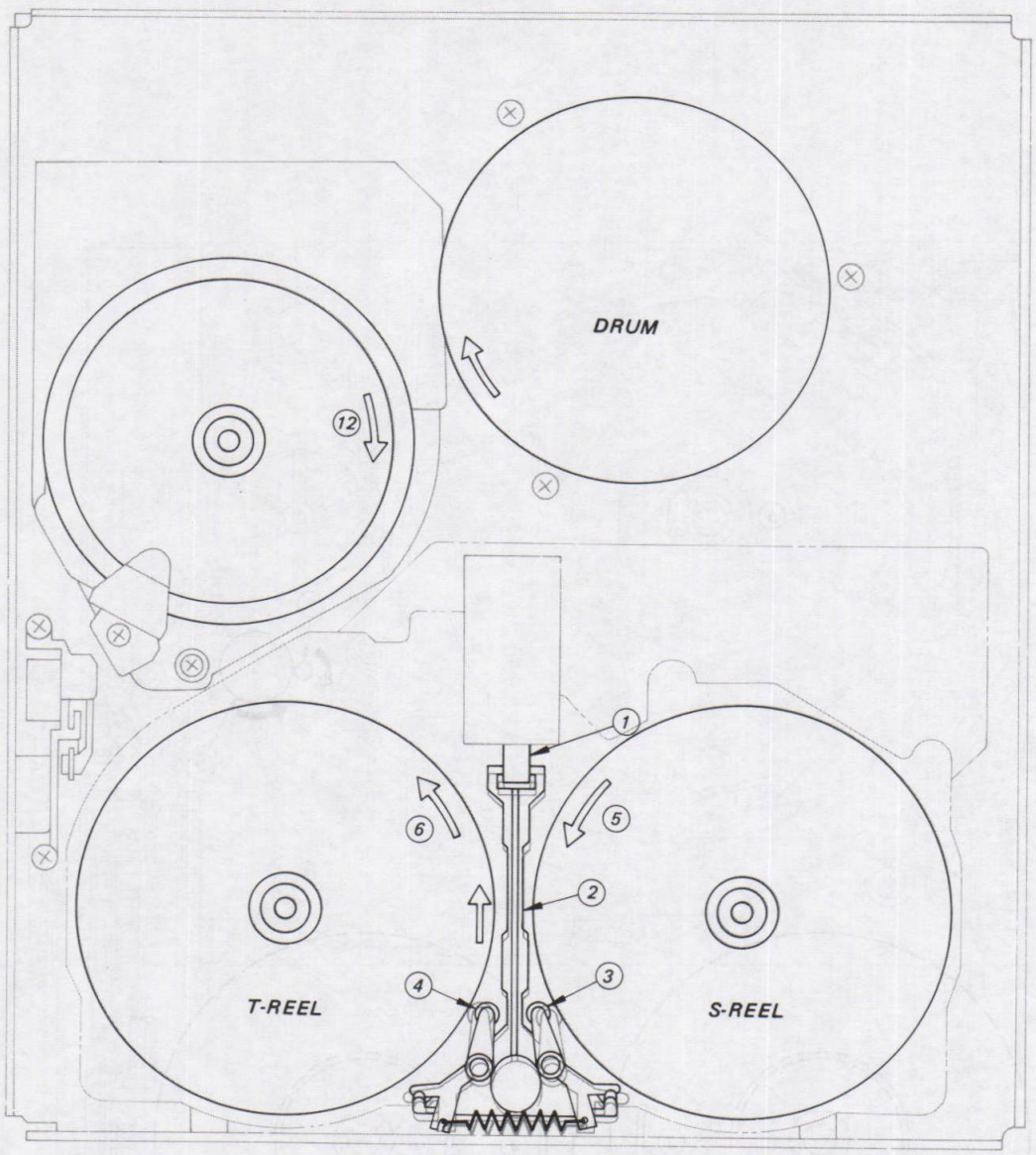
Fig. 8-12a.

arrow ⓐ. This pushes pinch roller arm ⑪ in the direction of arrow ⓑ, and pinch roller ⑬ rotates in the direction of arrow ⓒ according to the rotation of capstan motor shaft ⑫.

If the erase prevention tab on the back of the cassette is broken, the cassette does not push MR probe ⑭, so microswitch ⑮ does not operate, and REC mode is not obtained even when the REC button is pressed.

As shown in Fig. 8-12, when the switch operates, the cassette pushes MR probe ⑭ down and MR arm ⑯ rotates around shaft Ⓐ in the direction of arrow ⓓ.

Section Ⓑ arm rises, opening the point of contact ⑰ with microswitch ⑮, the switch goes off, and REC mode can be obtained.



BOTTOM VIEW

Fig. 8-13.

8-7. PICTURE

8-7-1. FORWARD PICTURE SEARCH (CUE)

Figs. 8-14, 15 show the mechanical operation during speed search (CUE) mode.
When FF button is pressed during PLAY mode, capstan motor shaft (1) and pinch roller (2) rotate faster than during PLAY mode causing the tape to mvoe faster. The result is a hi-speed picture (approximately 9 times faster for βII recording and 15 times faster for βIII recording). Take-up reel (4) rotation speeds up, as does supply reel (3) rotation. The drum (5) rotates at the same speed as during PLAY mode.

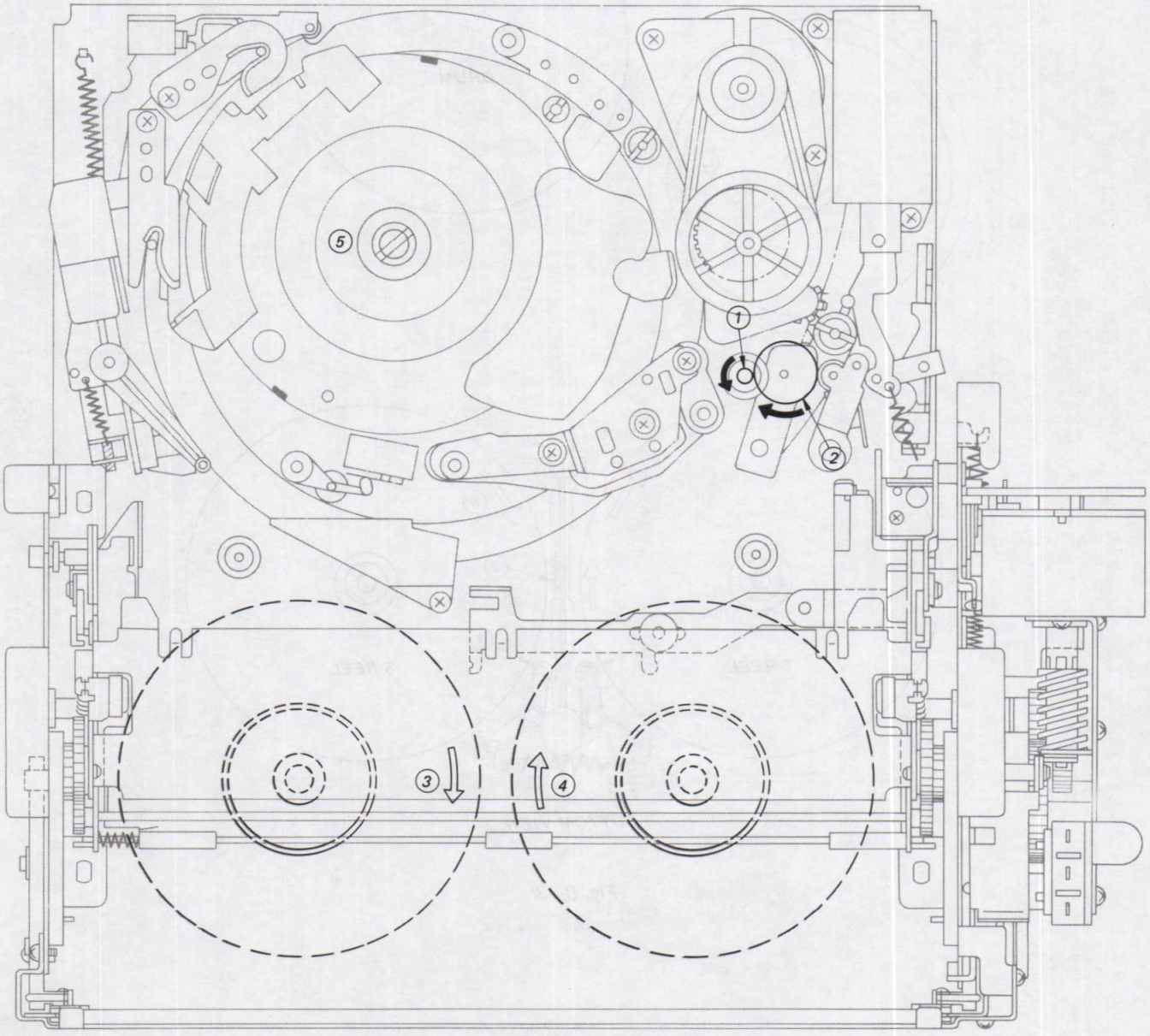
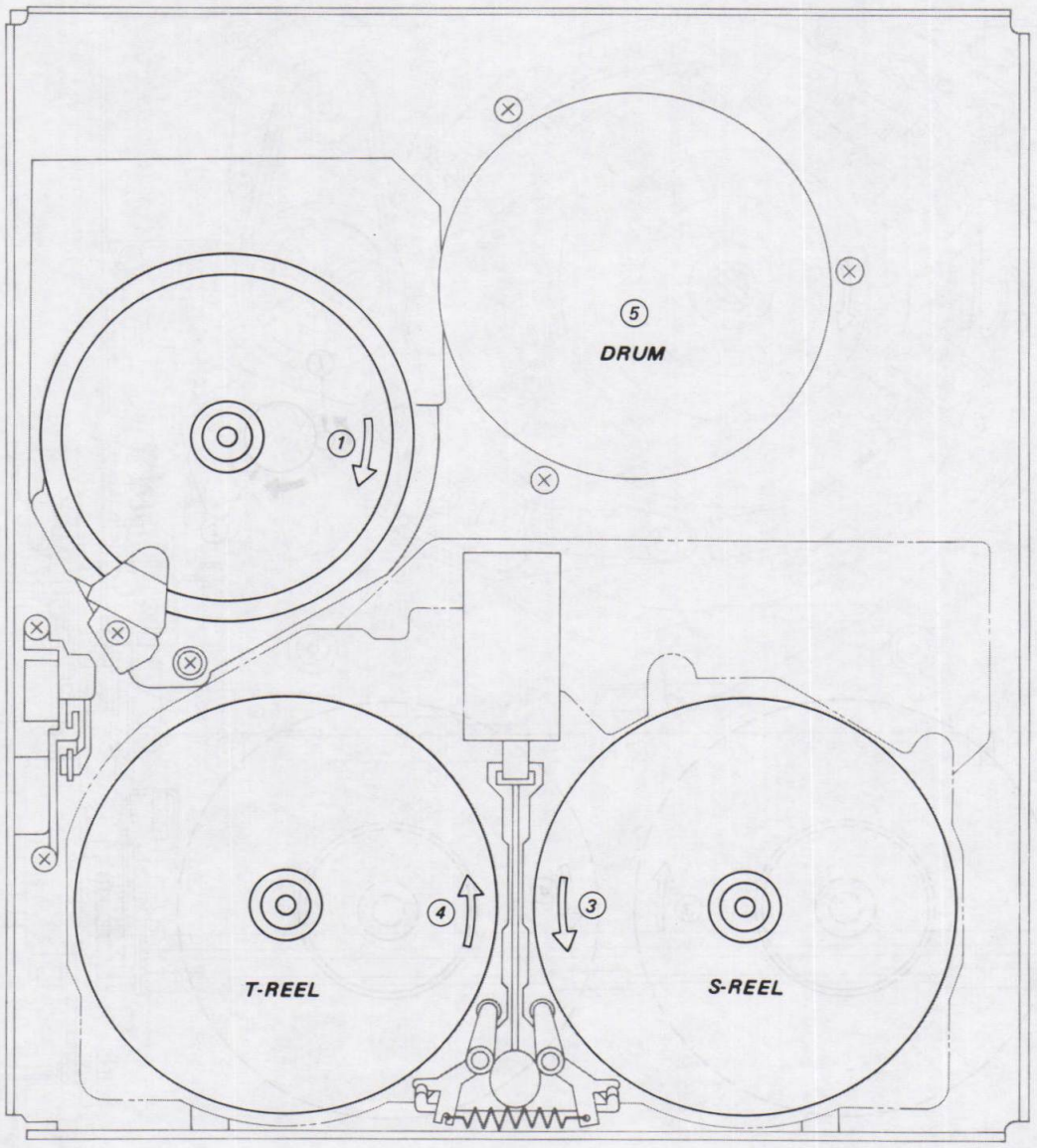


Fig. 8-14.



BOTTOM VIEW

Fig. 8-15.

8-7-2. REVERSE PICTURE SEARCH (REVIEW)

Figs. 8-16, 17 show the mechanical operation during reverse speed search mode.
When REW button is pressed during PLAY mode, capstan motor shaft ① and pinch roller ② begin to rotate in the opposite direction from PLAY mode rotation. Their rotation speed is the same as for forward picture search mode, and supply reel ③ rotates faster than during PLAY mode, as does take-up reel ④. However, take-up reel ④ motor rotates in the same direction as for PLAY mode, and slightly faster, in order to prevent tape slackness during reverse speed search.

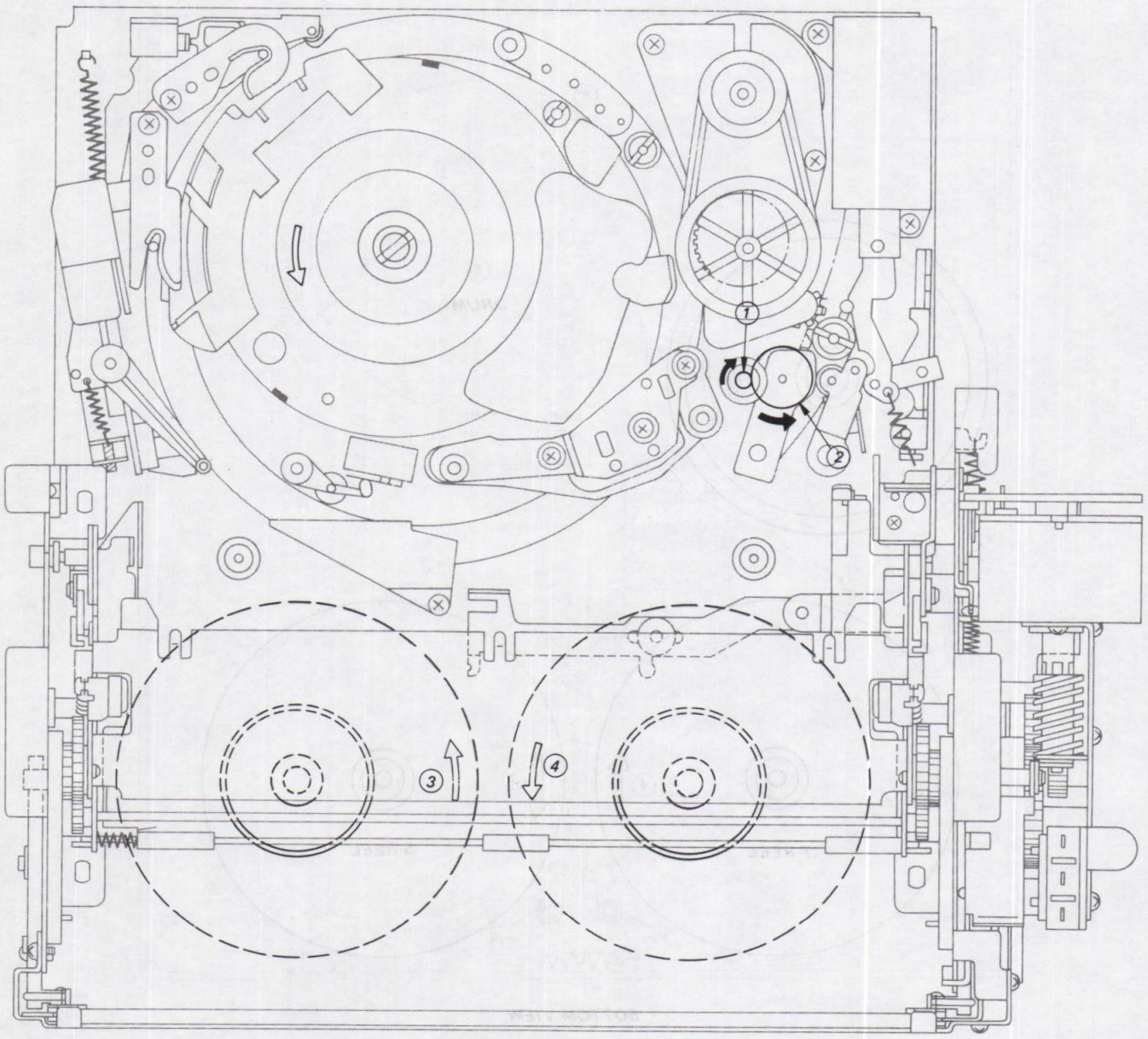
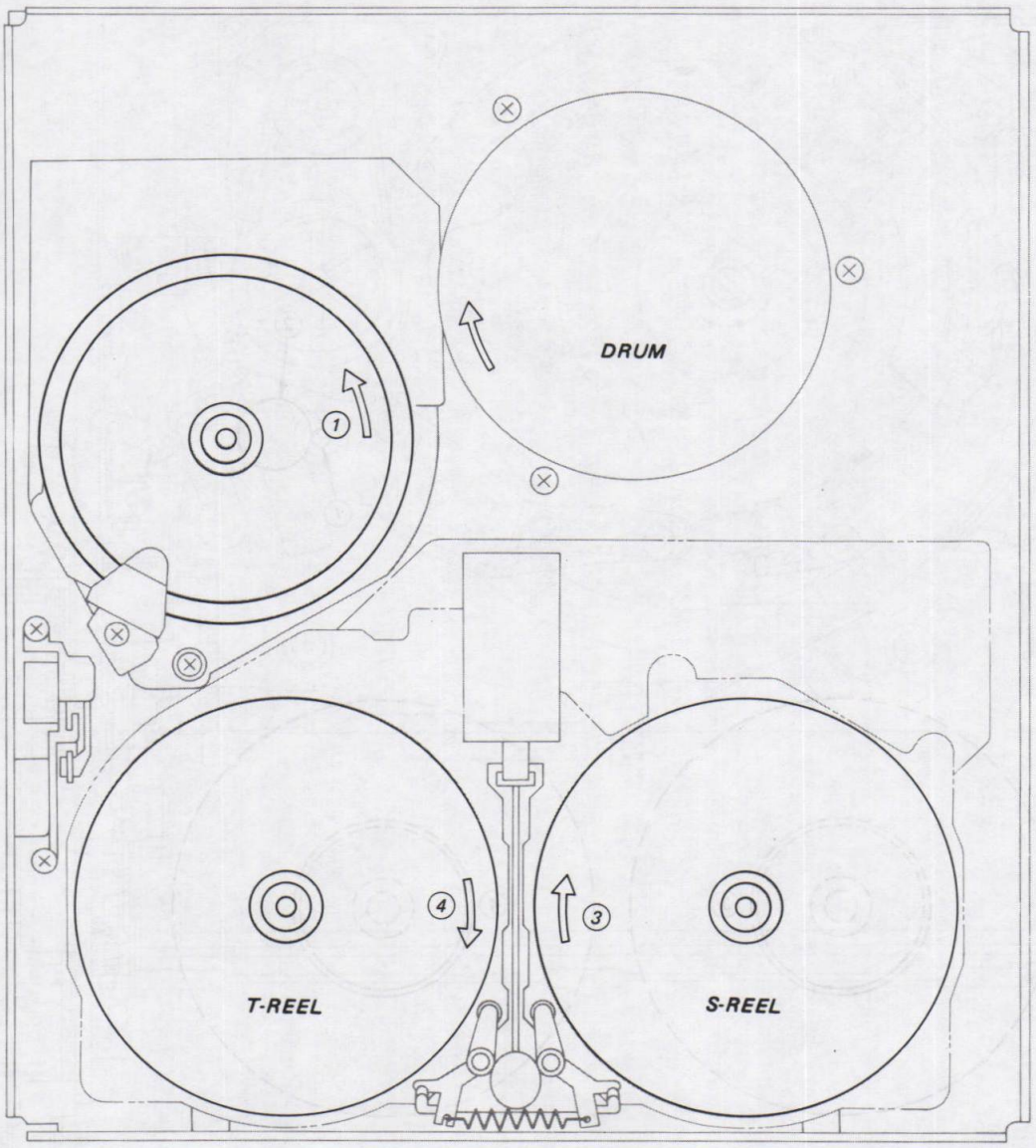


Fig. 8-16.



BOTTOM VIEW

Fig. 8-17.

8-8. PAUSE MODE

Fig. 8-18 shows the mechanical operation during PAUSE mode. This mode operates only for PLAY, REC or DUB mode. Capstan motor shaft (1) and pinch roller (2) stop rotating. Supply reel (3) and take-up reel (4) also stop rotating, but this does not mean that the reel motors are being braked. Supply reel (3) and take-up reel (4) are moving in the opposite direction from each other, but tape tension stops them. The tape remains in contact with the drum and stops, and a still image is produced.

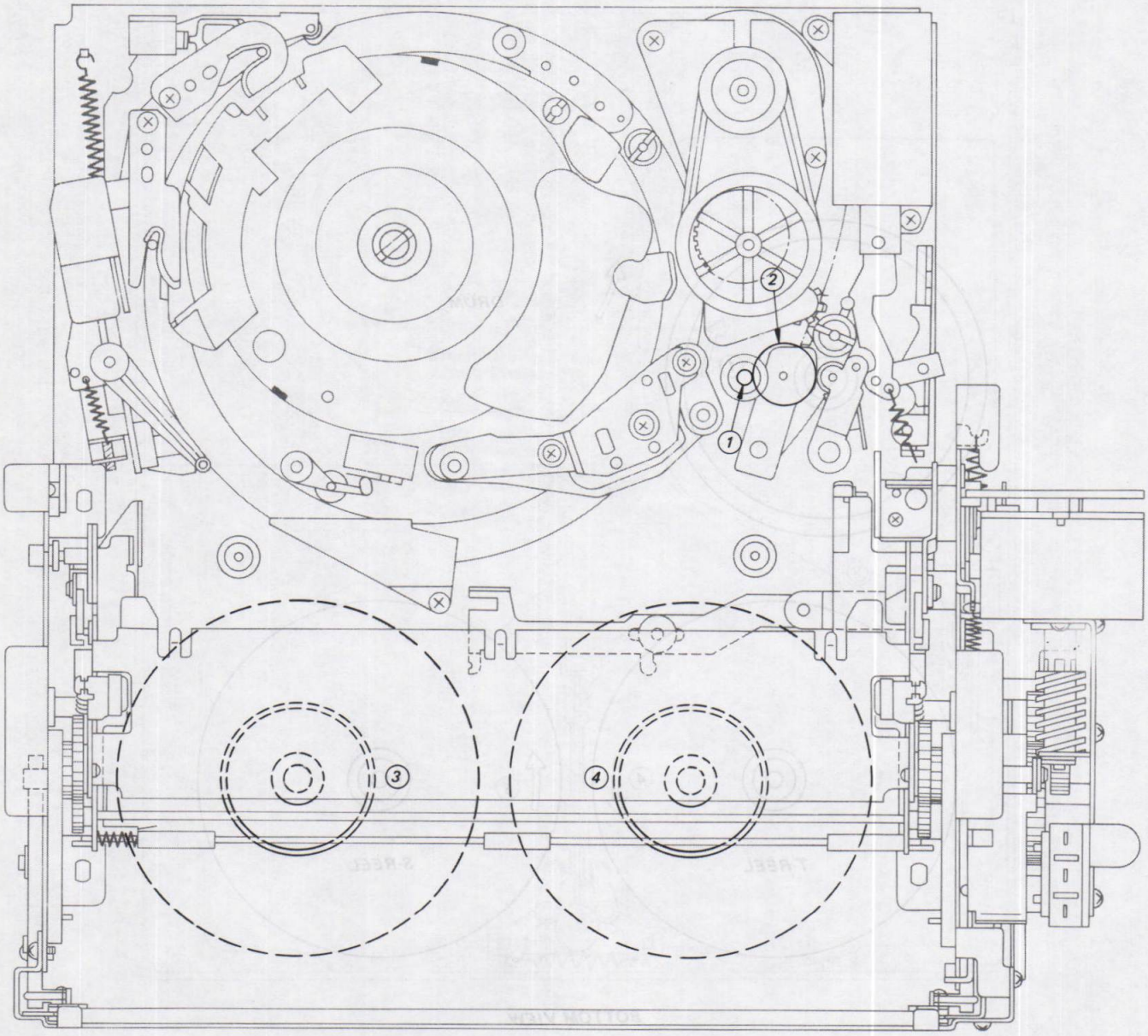


Fig. 8-18.

8-9. SPEED CONTROL

A speed control mode results when the each SPEED CONTROL button is pressed during PLAY mode. This cannot be done in any mode other than PLAY mode. Fig. 8-19 shows the forward operations of each SPEED CONTROL mode. There is a picture but no audio for each mode. Capstan motor (1), pinch roller (2), supply reel (3) and take-up reel (4) rotate in the same direction as for PLAY mode, and the speed is different for each mode.

Fig. 8-21 shows the reverse operation for each SPEED CONTROL mode. Picture, audio and rotation speedsa re the same as for forward operation, but rotation directions are opposite.

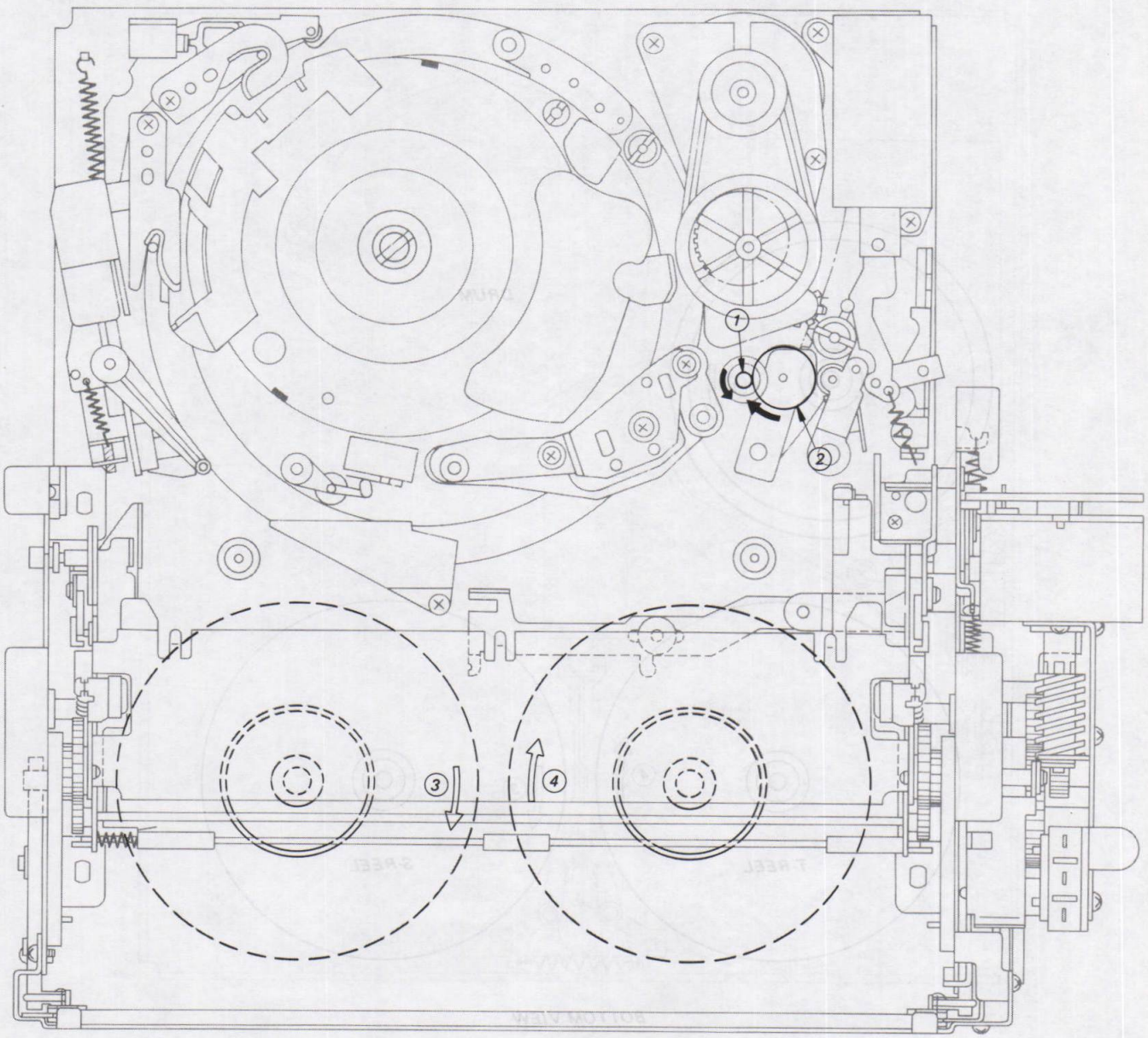
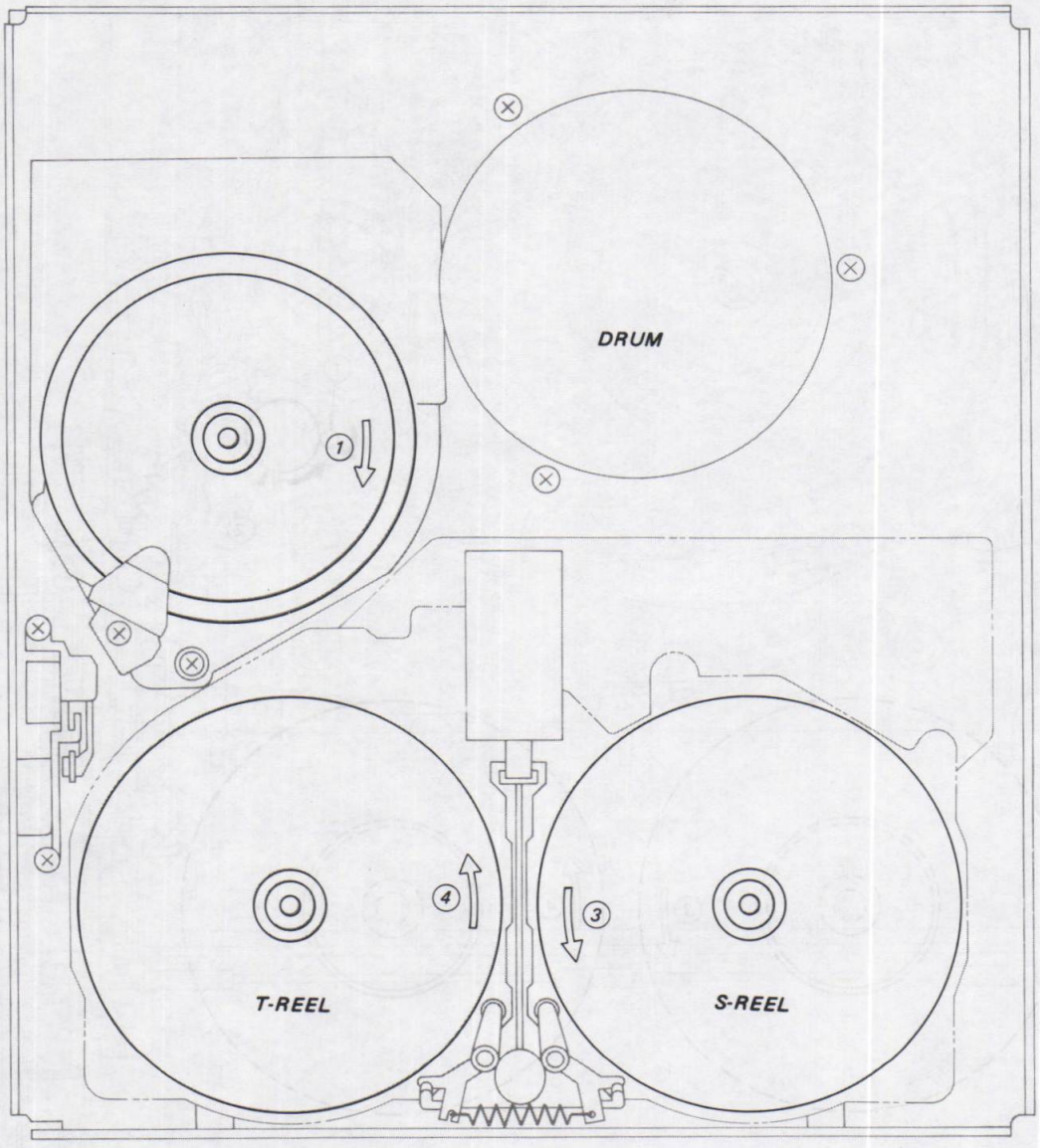


Fig. 8-19.



BOTTOM VIEW

Fig. 8-20.

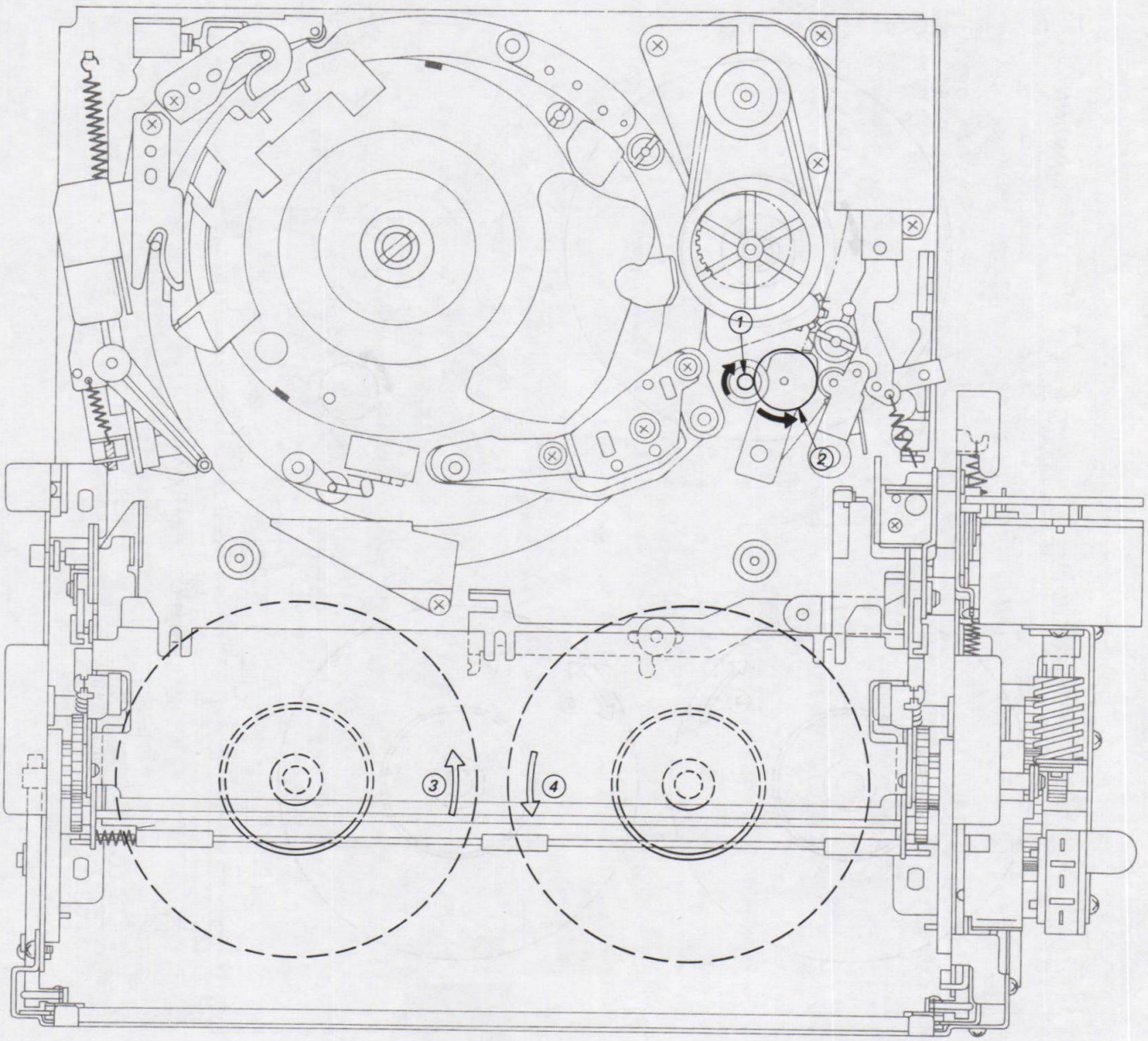


Fig. 8-21.

8-10. GO TO ZERO (MEMORY STOP)

GO TO ZERO rewinds the tape or moves it fast forward until the counter is set at 0. The zero set button is pressed to set the counter at zero, but this will also occur if power is cut.

Figs. 8-22, 23 show the mechanical operation of GO TO ZERO. When GO TO ZERO button is pressed, brake solenoid (1) is energized, supply brake (2) and take-up brake (3) are released, and supply reel (4) and take-up reel (5) begin to rotate. The tape either rewinds or moves fast forward until the counter setting reaches 0.

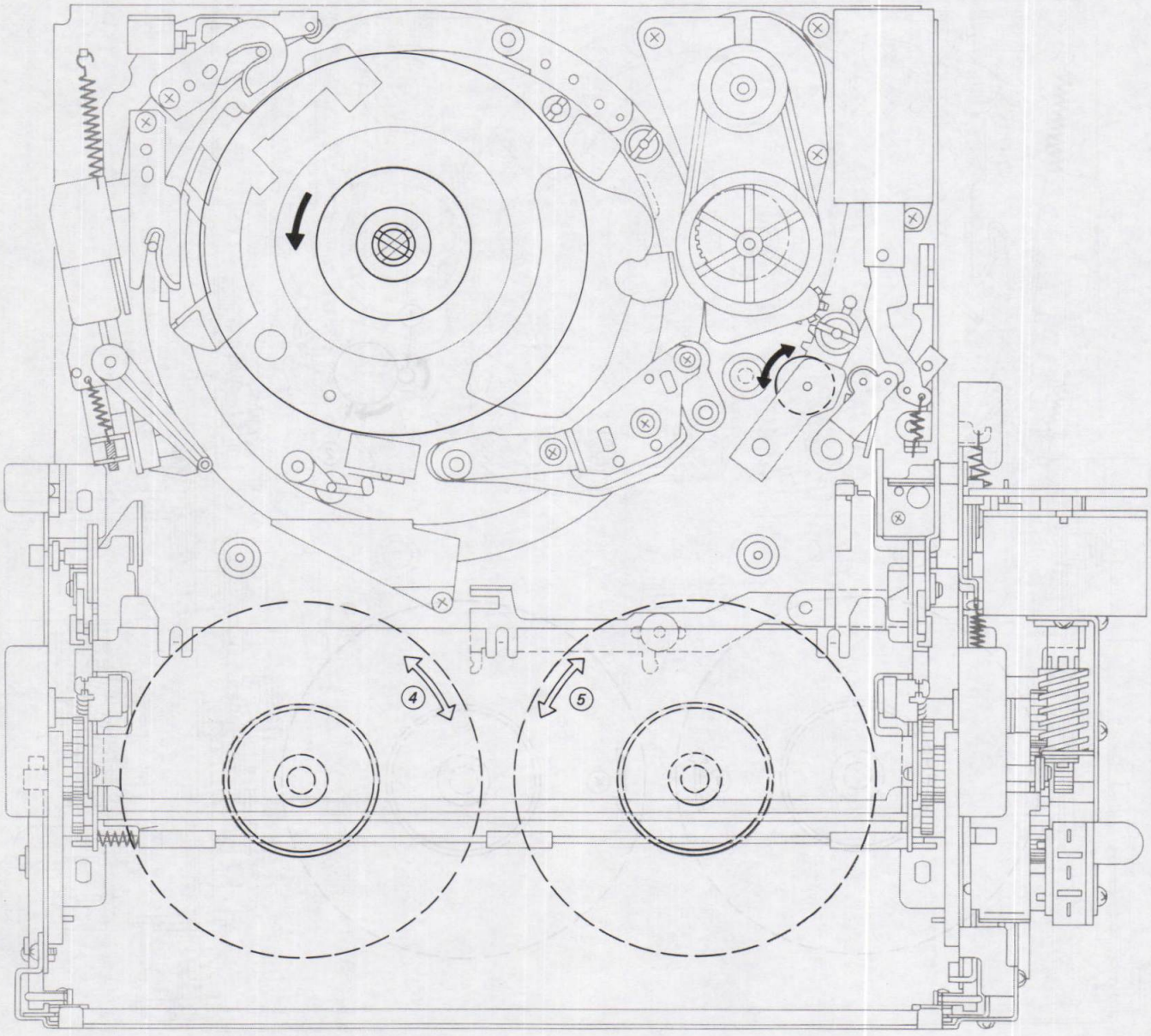
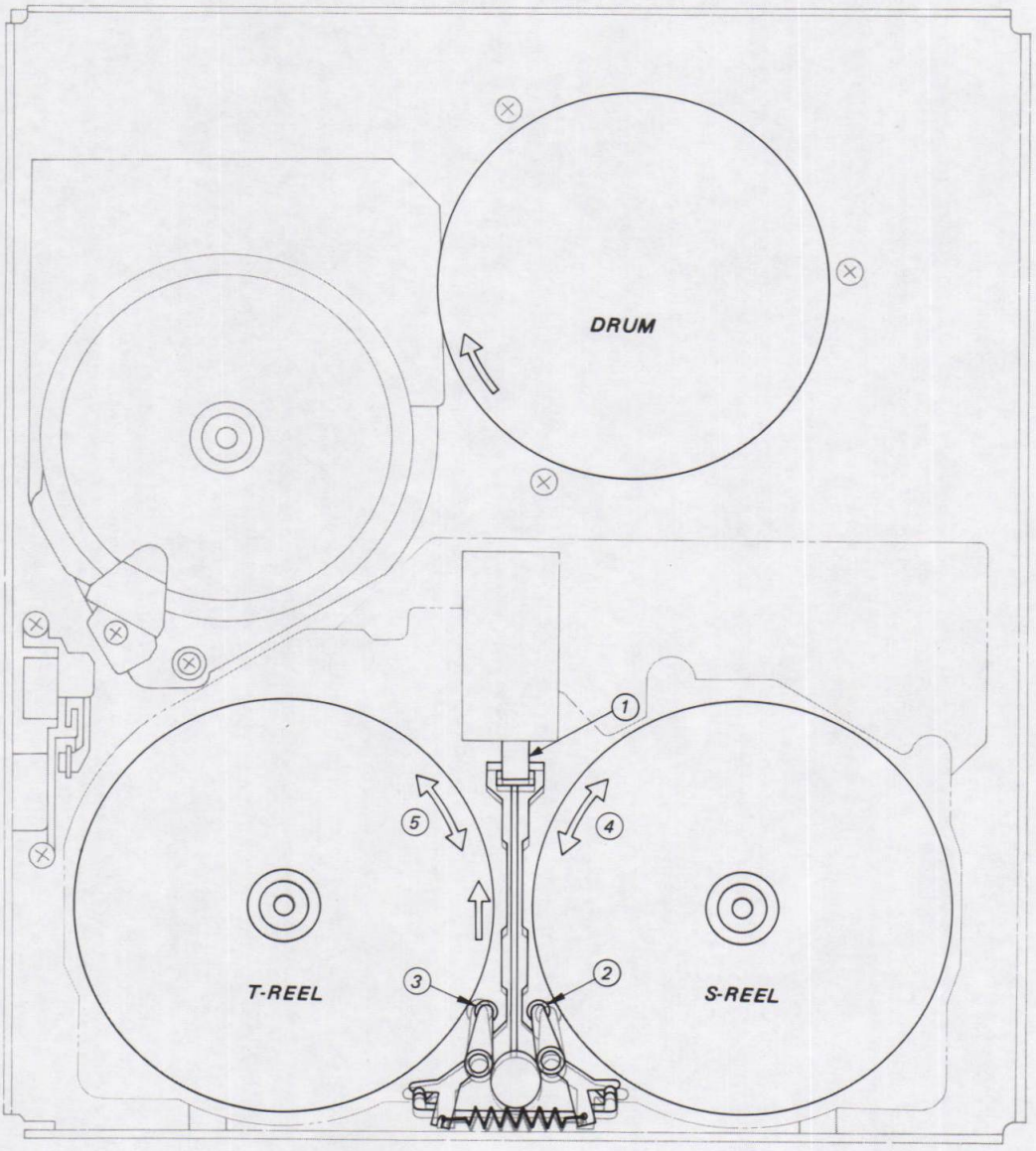


Fig. 8-22.



BOTTOM VIEW

Fig. 8-23.

8-11. AUDIO DUB MODE

To set the system to the AUDIO DUB mode, select the AUDIO DUB CH-1, 2/L, R mode by depressing the AUDIO DUB CH-1, 2/L, R key in the STOP state.
When the CH-2/R key is depressed, the system is set to the AUDIO DUB CH-2/R mode.
The mechanical operation during the AUDIO DUB mode is the same as in record mode. (See page 176.)

8-12. EJECT

Figs. 8-24, 25, 26 show the mechanical operation of cassette EJECT. When the EJECT button is pressed, threading motor (1) rotates in the direction of the arrow. This rotation is transmitted to gear pulley (3) via belt (2), and gears D (4) and F. (5) rotate respectively in the directions of the arrows.

The rotation of gear D (4) causes S-threading ring (6) to rotate in the direction of the arrow, and the rotation of gear F (5) causes slider gear assembly (7) to move in the direction of the arrow.

The rotation of S-threading ring (6) causes the cut out part of section A to move, so lock arm assembly (8) is pushed in the direction of the arrow and TP assembly (9) also moves in the direction of the arrow. Roller (11) on unthreading end switch arm (10) drops into the indentation of section (B), and the unthreading end switch (12) actuater moves in the direction of the arrow, turning unthreading end switch (12) off. With the movement of S-threading ring (6) and slider gear assembly (7), brake solenoid (13) is energized and supply brake (14) and take-up brake (15) are released. Supply reel (16) rotates and takes up the tape. Slider gear assembly (7) pushes section (C) of unlock plate (17), moving unlock plate (17) and unlock link plate 18 in the direction of the arrow. Unlock level (19) rotates in the direction of the arrow. This causes lock plate (20) to move and section (D) lock is released. CD adjust plate (21) also moves in the same direction as lock plate (20), microswitch (22) turns off, thread-

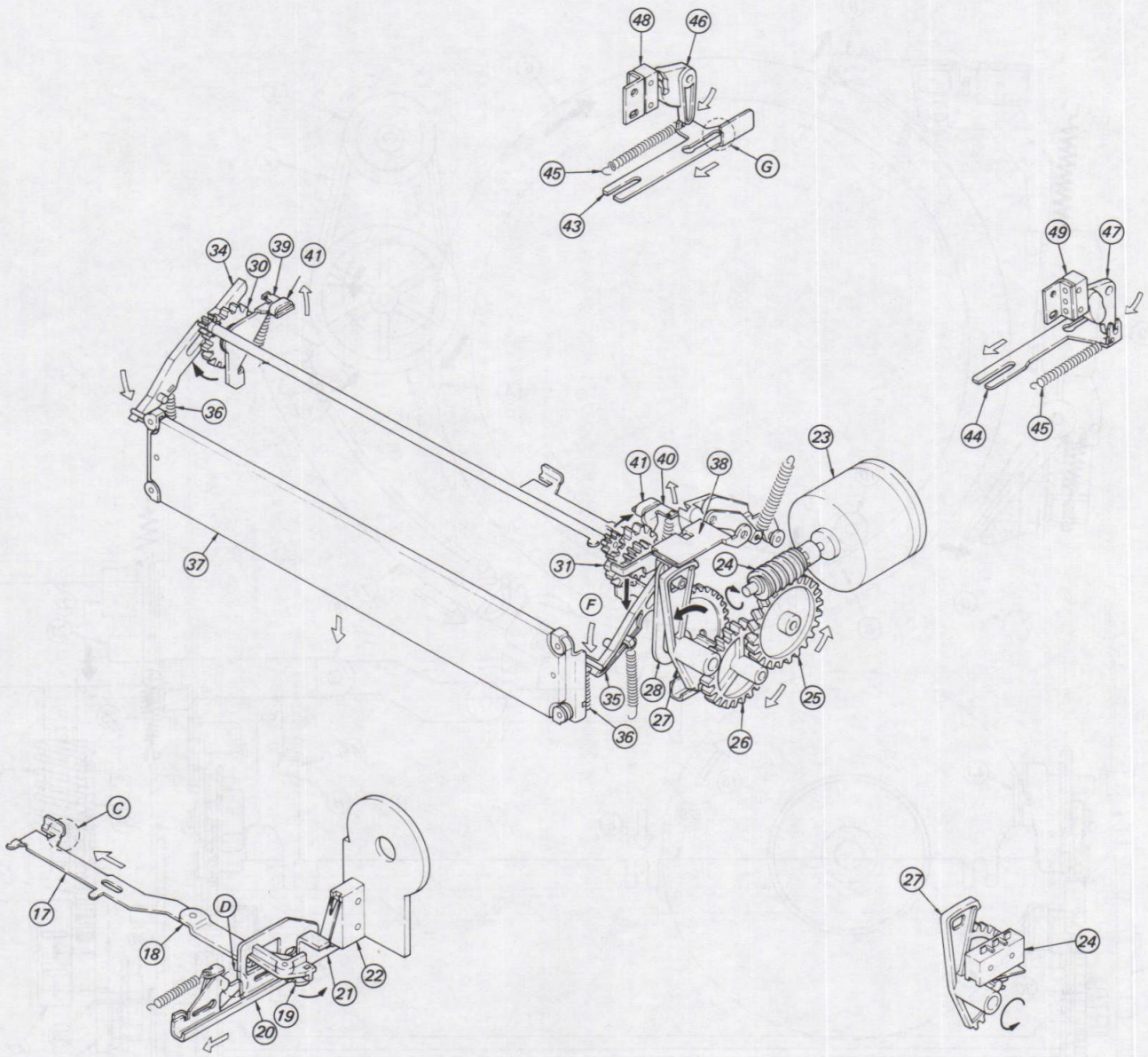


Fig. 8-24.

ing motor (1) stops and FL motor (23) turns on. Worm gear (24), worm wheel (25) and gear A (26) rotate respectively in the directions of the arrows. Sector gear (27) and holder drive arm (28) which are engaged with gear A (26) rotate in the direction of the arrow, and cassette compartment assembly (29) begins to move in the direction of arrow (E).

Gears E (30) and B (31) on cassette compartment assembly (29) rotate respectively along rack (L) (32) and rack (R) (33) and cassette compartment assembly (29) is set in position.

As cassette compartment assembly (29) moves in the direction of arrow E, door arm (L) (34) and arm (R) (35) are lowered in the direction of the arrow by tension coil spring (36), and cassette door assembly (37) is lowered in the direction of the arrow.

As cassette compartment assembly (29) nears its final position, sector gear (27) pushes UP lock arm (38) up. Cassette holder (L) (39) and (R) (40) rise in the direction of the arrow, and cushion (41) which is holding the cassette is released. Simultaneously, UP lock arm (38) drops in the direction of arrow (F), locking sector gear (27), and microswitch (42) turns off.

When cushion (41) is released, C slide plate (L) (43) and plate (R) (44) are moved in the direction of the arrow by tension coil spring (45). C-IN cam (L) (46) and (R) (47) rotate in the directions of the arrow, microswitches (48), (49) turn off and FL motor (23) stops.

The cassette is pressed against sections (G), (H) and comes out automatically.

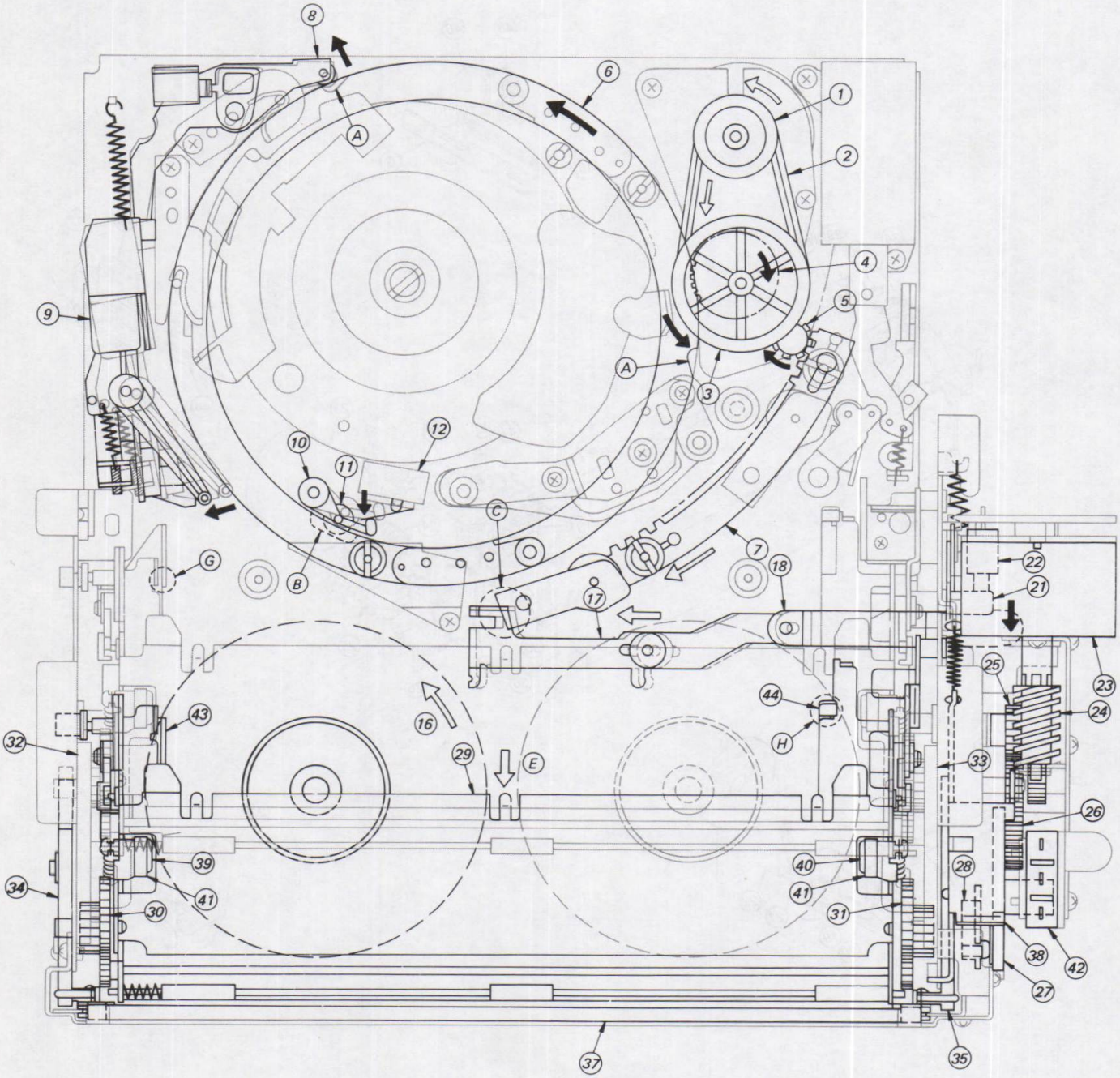
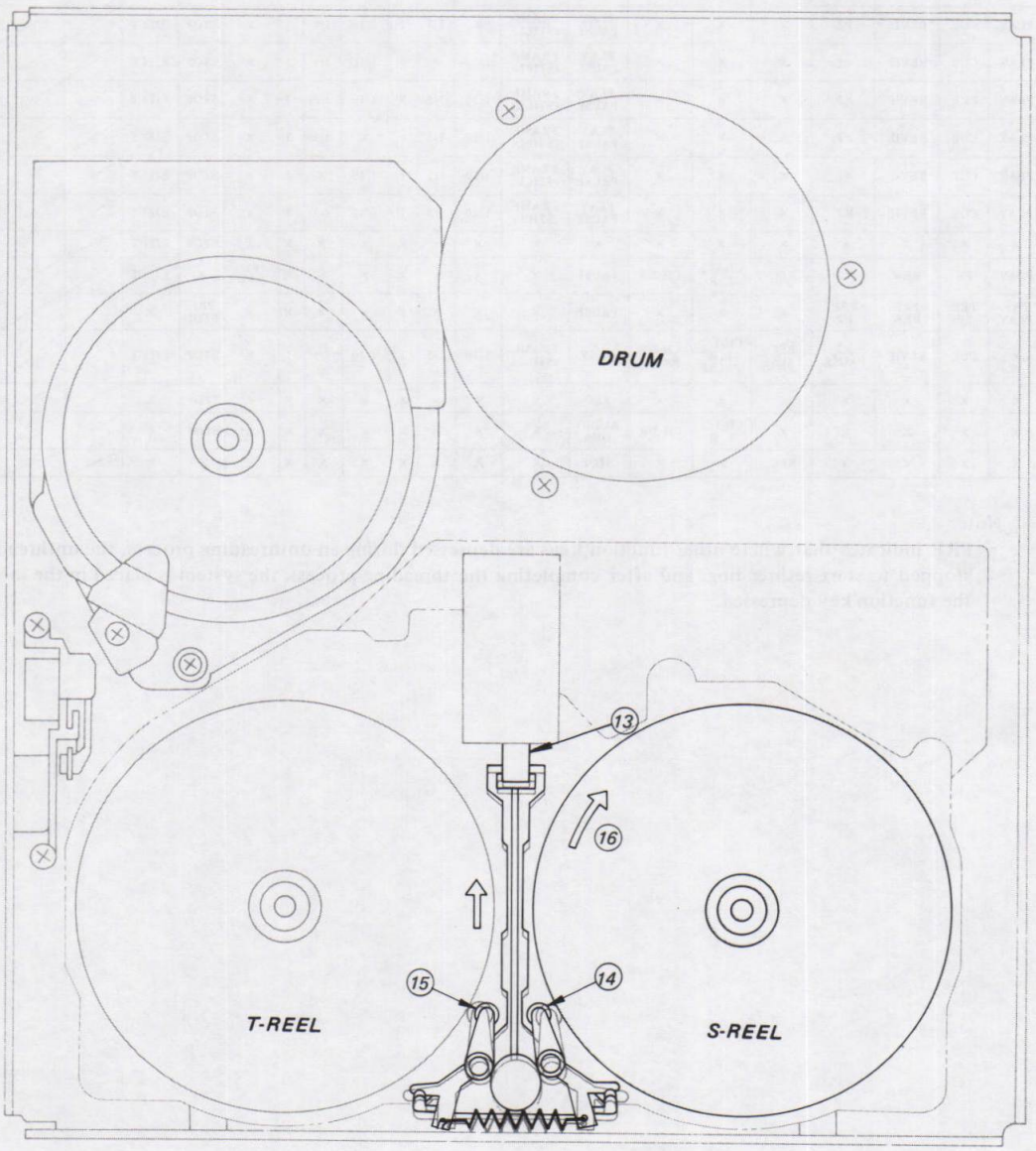


Fig. 8-25.



BOTTOM VIEW

Fig. 8-26.

Function Key (Mode) Matrix Table

Change Mode / Present Mode	▶ PLAY	▶▶ FF	◀◀ REW	◀ PLAY X2	● REC	▬ AUDIO DUB CH-1, 2 L,R	▬ AUDIO DUB CH-2 R	⏸ PAUSE	FRAME (STILL)	◁ 1/10	◁ 1/5	◁ 1	▷ 1/10	▷ 1/5	▷ 1	GO TO ZERO	■ STOP	⏏ EJECT	PLAY PAUSE	REC PAUDE	AUDIO DUB PAUSE	PAUSE
PLAY ▶	x	CUE	REVIE	x2	x	x	x	PLAY PAUSE	FRAME (STILL)	1/10	1/5	1	1/10	1/5	1	x	STOP	EJECT				
FF ▶▶	PLAY	x	REW	x2	x	x	x	x	x	x	x	x	x	x	x	x	STOP	EJECT				
REW ◀◀	PLAY	FF	x	x2	x	x	x	x	x	x	x	x	x	x	x	x	STOP	EJECT				
PLAY X2 ◀	PLAY	CUE	REVIE	x	x	x	x	X2 PAUSE	FRAME (STILL)	1/10	1/5	1	1/10	1/5	1	x	STOP	EJECT				
REC ●	x	x	x	x	x	x	x	REC PAUSE	x	x	x	x	x	x	x	x	STOP	x				
▬ AUDIO DUB CH-1, 2/L, R	x	x	x	x	x	x	x	CH-1, 2 L, R PAUSE	x	x	x	x	x	x	x	x	STOP	x				
▬ AUDIO DUB CH-2/R	x	x	x	x	x	x	x	CH-2/R PAUSE	x	x	x	x	x	x	x	x	STOP	x				
FRAME (STILL)	PLAY	CUE	REVIE	X2	REC PAUSE	CH-1, 2 L, R PAUSE	CH-2/R PAUSE	PLAY PAUSE	x	1/10	1/5	1	1/10	1/5	1	x	STOP	EJECT				
◁ 1/10	PLAY	CUE	REVIE	X2	x	x	x	PLAY PAUSE	FRAME (STILL)	x	1/5	1	1/10	1/5	1	x	STOP	EJECT				
◁ 1/5	PLAY	CUE	REVIE	X2	x	x	x	PLAY PAUSE	FRAME (STILL)	1/10	x	1	1/10	1/5	1	x	STOP	EJECT				
◁ 1	PLAY	CUE	REVIE	X2	x	x	x	PLAY PAUSE	FRAME (STILL)	1/10	1/5	x	1/10	1/5	1	x	STOP	EJECT				
▷ 1/10	PLAY	CUE	REVIE	X2	x	x	x	PLAY PAUSE	FRAME (STILL)	1/10	1/5	1	x	1/5	1	x	STOP	EJECT				
▷ 1/5	PLAY	CUE	REVIE	X2	x	x	x	PLAY PAUSE	FRAME (STILL)	1/10	1/5	1	1/10	x	1	x	STOP	EJECT				
▷ 1	PLAY	CUE	REVIE	X2	x	x	x	PLAY PAUSE	FRAME (STILL)	1/10	1/5	1	1/10	1/5	x	x	STOP	EJECT				
GO TO ZERO	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	STOP	EJECT				
STOP ■	PLAY	FF	REW	X2	REC	CH-1, 2 L, R	CH-2/R	PAUSE	x	x	x	x	x	x	x	FF REW	x	EJECT				
※ EJECT ⏏	PRE PLAY	PRE FF	PRE REW	PRE X2	x	x	x	PAUSE	x	x	x	x	x	x	x	x	PRE STOP	x				
⏸ PLAY PAUSE	x	CUE	REVIE	X2 PAUSE	REC PAUSE	CH-1, 2 L, R PAUSE	CH-2/R PAUSE	PLAY	FRAME (STILL)	1/10	1/5	1	1/10	1/5	1	x	STOP	EJECT				
⏸ REC PAUSE	x	x	x	x	x	x	x	REC	x	x	x	x	x	x	x	x	STOP	x				
⏸ AUDIO DUB PAUSE	x	x	x	x	x	CH-1, 2 L, R	CH-2/R	AUDIO DUB	x	x	x	x	x	x	x	x	STOP	x				
⏸ PAUSE	x	x	x	x	REC	x	x	STOP	x	x	x	x	x	x	x	x	x	x				

Note:

※ PRE indicates that where other function keys are depressed during an unthreading process, the unthreading process is stopped to start rethreading, and after completing the threading process, the system is placed in the mode relating to the function key depressed.

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